

Downloading CPLDs with an Embedded Processor

With its FastFLASH™ technology supporting up to 10,000 program/erase cycles, Xilinx XC9500 CPLDs bring all the advantages of in-system programming (ISP) to an advanced CPLD architecture. Embedded processors can be used to control CPLD in-system programming, resulting in considerable benefits throughout the product life cycle, from initial design to field updates.

Why embedded downloading?

Generally, designers download their CPLD patterns through a serial port driven from a PC or workstation during system development and debug. Once the design is stable and high-volume production

the case of CPLD devices, the most-frequently used access port is the JTAG boundary scan interface (that same port can provide “double duty” as both a programming and test access port).

With the embedded processor controlling the JTAG interface, the board’s CPLDs can be reconfigured by providing new programming information to the processor. As a result, changes can be easily implemented during design, prototyping, manufacturing or in the field. With sufficient prior planning, extensive design changes can be implemented (if needed) without making external physical changes in the system, such as modifications to the printed circuit board — perhaps even without opening the system enclosure!

This approach allows changes after field installation with minimal risk to overall system behavior. End users can update their own hardware. For systems with a floppy disk or CD drive, field upgrades can be implemented just like a software update. Remote updating is possible using a modem or other communication link — the embedded controller would capture update information from an external data stream and channel it to the ISP CPLDs on the board, as well as on-board flash memories (or volatile memories).

The non-volatile XC9500 CPLDs do not need reloading with each power cycle. However, because they can coexist in the same JTAG download chain with FPGAs, it may be easier and more convenient to reload their configurations during every power-up sequence. The 10,000 reprogramming cycles offered by XC9500 CPLD FastFLASH™ technology makes that strategy possible. By using the advanced JTAG capabilities contained in the XC9500 devices, the internal UserCode register can maintain a reprogramming counter, if needed.

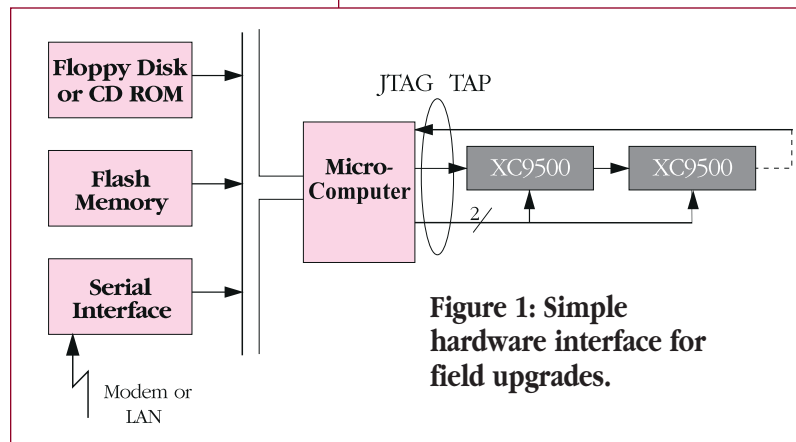


Figure 1: Simple hardware interface for field upgrades.

begins, production-level programming can be switched to third-party programmers (such as those from Data I/O and BP Microsystems) or third-party ATE systems (such as those from HP, GenRAD and Teradyne). Increasingly, however, designers need to program parts directly using the onboard microprocessor in an embedded system.

Having the microprocessor handle design changes on its “own” board fits the “embedded” paradigm. Embedded systems should be designed with a single, unified information port for the programming of all reconfigurable devices on the board. In

Keeping Up with Changing Standards

There are many benefits to embedded in-system programming. Products can be updated to the "leading edge" just before shipping and then updated in the field as technology changes, rather than wait to ship until all expected upgrades are complete. For example, this capability could allow a manufacturer to ship products based on new and evolving standards because once a standard has been established, previously shipped systems can be updated in the field to maintain compliance (see **Figure 1**).

To accommodate potential field upgrades, choose a CPLD device with a robust architecture to ensure that ample speed and capacity are available to tolerate future changes. The XC9500 architecture is specifically designed to tolerate a wide range of changes while retaining the pinouts initially dictated by the PCB design. By choosing the right XC9500 device and including embedded programming capabilities in the system, embedded download success is assured.

Embedded Download App Note

Xilinx has developed the tools needed to deliver this powerful capability to designers. The package includes a thoroughly tested, transportable C program, a detailed application note on its use, and the Xilinx EZTag™ software. The design was initially developed for an 80C51-type microcontroller, but the processor-specific aspects are kept to a minimum, with a simple assembler level call. This keeps all JTAG protocols at the fully transportable ANSI C level, for which there is an abundance of available compilers. The package covers all the necessary details, including the conversion of intermediate files to formats compatible with EPROM programmers.

To obtain the embedded download application note and software, simply access the WebLINX web site at www.xilinx.com and look for the CPLD applications section. Alternately, make your request via e-mail to isp@xilinx.com. ♦

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