

# 1997 *The Year That Defines the Future*

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In 1985, Xilinx introduced the world's first FPGA device, creating an important new product category in the semiconductor industry. Since then, a steady stream of new, innovative component and development system products has allowed Xilinx to grow into the industry's leading supplier of programmable logic.

In 1997, the pace of innovation will increase. By aggressively applying architectural improvements and the latest process technologies, Xilinx will be setting new standards for FPGA capacity, performance, and cost-effectiveness. All 10 members of the new XC4000XL family will be available by mid-year. Based on 0.35  $\mu$  technology, this family provides usable logic gate densities ranging from 5,000 to 85,000 gates (about 500 to 7,500 "logic cells," where a logic cell consists of a 4-input look-up table and a register). These are true "logic gates," not the "combined logic and memory gates" metrics used by others to inflate their gate counts.

By mid-year, we expect to be sampling the first FPGA based on a 0.25  $\mu$  process, and we will be working with 0.18  $\mu$  technology by year-end. Our next-generation architecture also should be available by year-end, and is projected to reach densities of over 30,000 logic cells (about 400,000 logic gates) in 1998. Of course, correspondingly faster speed grades also will be introduced, reaching true 100 MHz chip-to-chip performance later this year. Our next-generation of place and route tools will support these new offerings.

The XC5200 series FPGAs also will be migrated to a 0.35  $\mu$  process this year. Die sizes for these cost-optimized devices will shrink to the point where they are "pad limited"; that is, the die size is constrained by the number of I/O pads required, not the logic gate density. When this occurs, traditional gate arrays will have no die size advantage and, therefore, no cost advantage over FPGAs. Lower FPGA costs will open new markets to programmable logic devices in applications such as Internet appliances, PC add-in cards, consumer electronics, automotive electronics and large household appliances.

The Xilinx CPLD product lines will benefit equally from aggressive process migration this year. The industry has adopted FLASH memory technology as the mainstream floating-gate technology, facilitating the migration of the FLASH-based XC9500 family down the process curve. Xilinx CPLDs will continue to be the lowest-priced in the industry, while offering the best routability and pin-locking capabilities of any available CPLD.

## Optimizing the Process

Advanced process technology is critical to providing leading-edge performance, density and cost-effectiveness. Xilinx is firmly committed to always having and using the most advanced IC fabrication processes available. One of the major advantages of being a "fabless" semiconductor company is the ability to form manufacturing partnerships with the process leaders at any point in time. An in-house staff of process engineers allows Xilinx to work with our fabrication partners to quickly bring new processes on-line.

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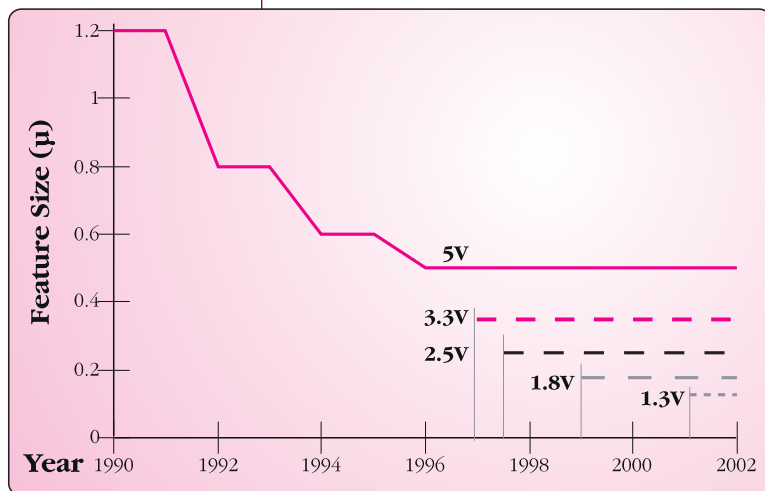
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The leading semiconductor foundries are eager to use Xilinx FPGAs to drive their process development. The regularity and testability of our FPGA architectures facilitates defect analysis and fault testing. With their large transistor counts (the XC4062XL device has about twice as many transistors as the Intel Pentium Pro processor), FPGAs are a very good "test vehicle" for the most-advanced fabrication lines.

### The Voltage Staircase

In order to reap the benefits of advancing process technology — increased performance, increased density, lower power consumption and lower price — users must be willing to migrate their designs down the "voltage staircase." The graph shows how CMOS process



**Rapidly shrinking device geometries will require the use of smaller supply voltages.**

technology has improved from 1.2  $\mu$  design rules in 1990 to today's 0.5  $\mu$  processes, while maintaining 5 volt logic levels. As geometries shrink below 0.5  $\mu$ , the smallest transistors cannot withstand 5 volts without damage. This leads to the voltage levels shown in the graph, with each successive process generation using a smaller supply voltage.

Xilinx is taking an active lead in working with our users to plan an orderly migration from one voltage standard to the next. A major part of our migration strategy is to maintain I/O compatibility across multiple generations. For example, all of the 3.3 V products in the XC5200L and XC4000XL families have I/O structures that are fully 5 V compatible —

accepting full 5 V signals on all I/Os and being able to drive TTL-like levels into any 5 V devices. Even our future 0.25  $\mu$ , 2.5 V components will employ split I/O and core power supplies to maintain I/O compatibility with either 5 V or 3.3 V devices.

This is not meant to imply that Xilinx will discontinue production of 5 V devices anytime soon. Although we encourage our users to migrate their designs to the lower voltage standards as these new products become available, we recognize that designs based on the 5 V standard will continue in production for many years to come, and we remain firmly committed to supporting those designs.

### Complete Solutions

Users require complete solutions that meet their logic requirements, not just the biggest or fastest device. We realize that programmable logic solutions consist of a combination of many elements, including device architecture, device packaging, EDA interface software, synthesis software, place and route implementation software, pre-designed cores, sales support, and technical support. We intend to continue to lead the market in all these areas.

In summary, Xilinx will be releasing a formidable array of new products in the coming year. These will include:

- The industry's highest-density FPGAs
- The fastest FPGAs
- The first full family of FPGAs available for 3.3 V systems
- The first FPGAs using a 0.25  $\mu$  process
- The next major release of the Xilinx development software
- A broad offering of pre-designed cores
- The introduction of the next-generation FPGA architecture.

This will set the stage for the next five years, during which FPGA speeds are expected to increase five-fold, and FPGA densities will increase to 150,000 logic cells (2 million logic gates). ♦