PRELIMINARY MANUAL

for

MODEL 2116A COMPUTER
VOLUME THREE

INPUT/OUTPUT SYSTEM
OPERATION

PRINTED: APRIL 1967

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd.)

LIST OF ILLUSTRATIONS

LIST OF TABLES

APPENDIX A

LIST OF ILLUSTRATIONS

SECTION I

INTRODUCTION

1-1. COMPUTER SYSTEM

1-2. The computer system (Figure 1-1) consists of the HP 2116A Computer, associated Input/Output devices, and the necessary interface logic and software.

1-3. The basic computer contains the facilities for control of up to 55 peripheral devices. Plug-in processor options are available for expansion of computer capabilities, and a wide range of Input/Output options are available. Refer to Volumes I and II for detailed information on the computer, and the available processor options, and to Volume IV for Programming information.

1-4. MANUAL CONTENTS

1-5. This preliminary manual contains a description of the Input/Output structure in Section II. Theory of Operation information and Logic Diagrams for the I/O Control card, the I/O Address card, and the Resistance Load card are contained in Sections III, IV and V respectively. Following Section V, the manual is divided into separate units according to Interface Kit accessory numbers. Each unit is divided into Sections and contains its own Table of Contents, List of Illustrations, and List of Tables. These units contain at least the following: 1) Operation information for the Input/Output device for which the Interface Kit provides the interface card and interconnecting cabling, and 2) Theory of Operation and Logic Diagrams for the interface card. Except for Operation information, detailed information on the Input/Output device is not provided. Complete Operating and Service manuals are provided for purchased Input/Output devices.

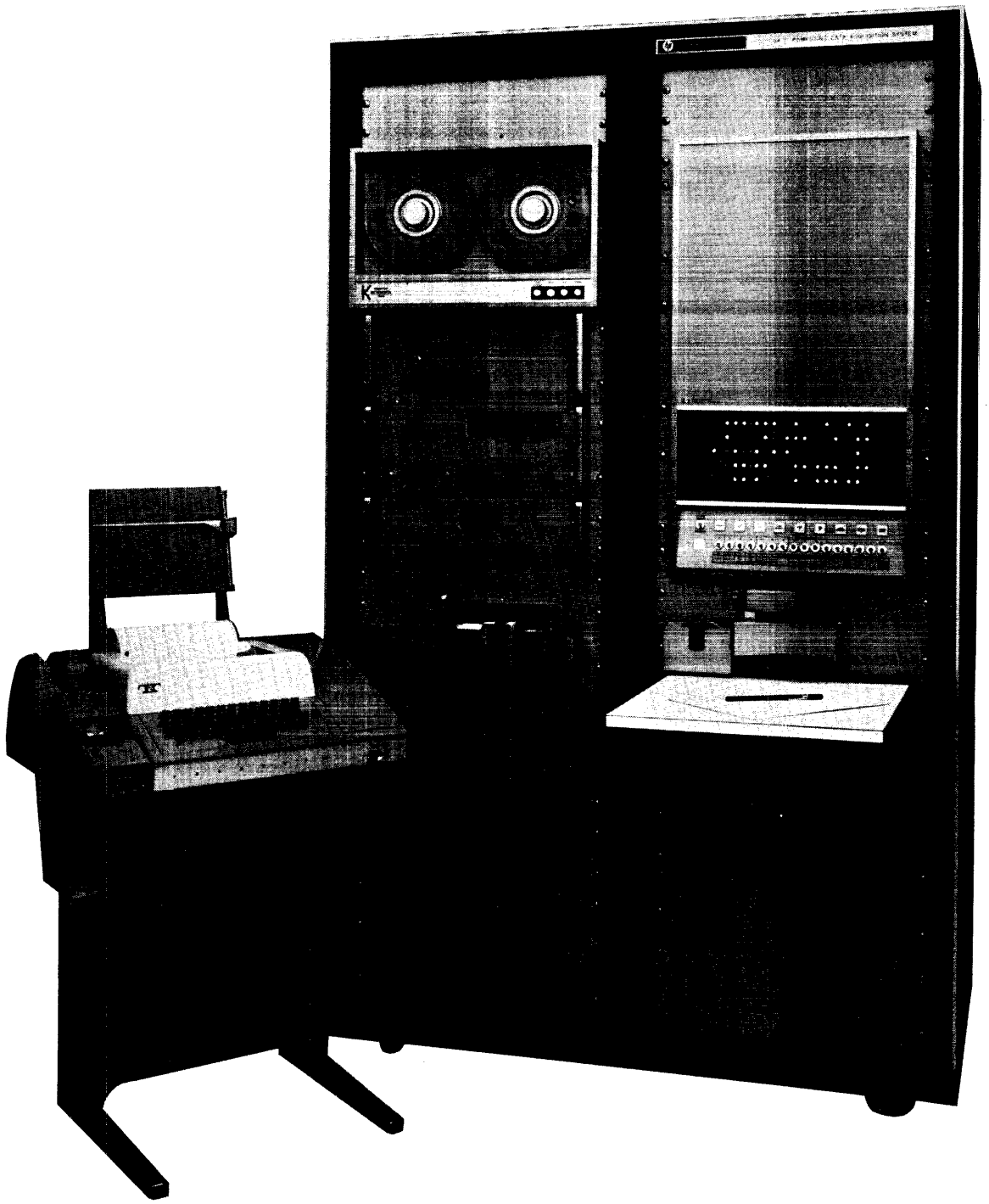


Figure 1-1. Typical HP 2116A Computer System

2-5. COMPUTER SYSTEM INPUT/OUTPUT OPERATIONS

2-6. GENERAL

2-7. Figure 2-2 illustrates the main elements of the computer system concerned with the control of Input/Output operations. All elements shown are contained in the computer main frame, except for the external devices. Although the R-, S-, and T-Buses are represented as single lines in Figure 2-2, each line is actually 16 individual lines. Also, interface arrangements are shown for only two external devices, one input and one output, where as many as 55 devices may exist. The elements illustrated process all Input/Output operations in two ways, as follows:

a. Processes Input/Output instructions.

b. Processes interrupt requests from the external devices.

2-8. INPUT/OUTPUT INSTRUCTIONS

2-9. Refer to Figure 2-2. Input/Output instructions from memory via the T-Register are decoded by the I-Register and routed to the various register gate inputs and to the Control Logic which translates the instructions into appropriate driving signals. Instruction Commands are routed to a particular interface card and external device as determined by the Select Code from the T-Register via the I/O Address card. These signals can set or reset the Control and Flag flip-flops (FFs) on the interface cards and can test the set or reset condition of these FFs. The Control and Flag FFs are used for transferring data between the interface card and the external device.

2-10. The IOI (I/O Input) signal strobes all interface cards for input data as a result of a Load Into A (LIA), Load Into B (LIB), Merge into A (MIA), or a Merge into B (MIB) instruction. Only the data from the interface card selected by the Select Code can be enabled. The data is strobed by the IOI signal onto the S-Bus. From there it is transferred via the Arithmetic Logic (to alter or combine the data) and the T-Bus to the A- or B-Register. The particular register which will receive the data is determined by the LIA/B or MIA/B signal present at the register input gate.

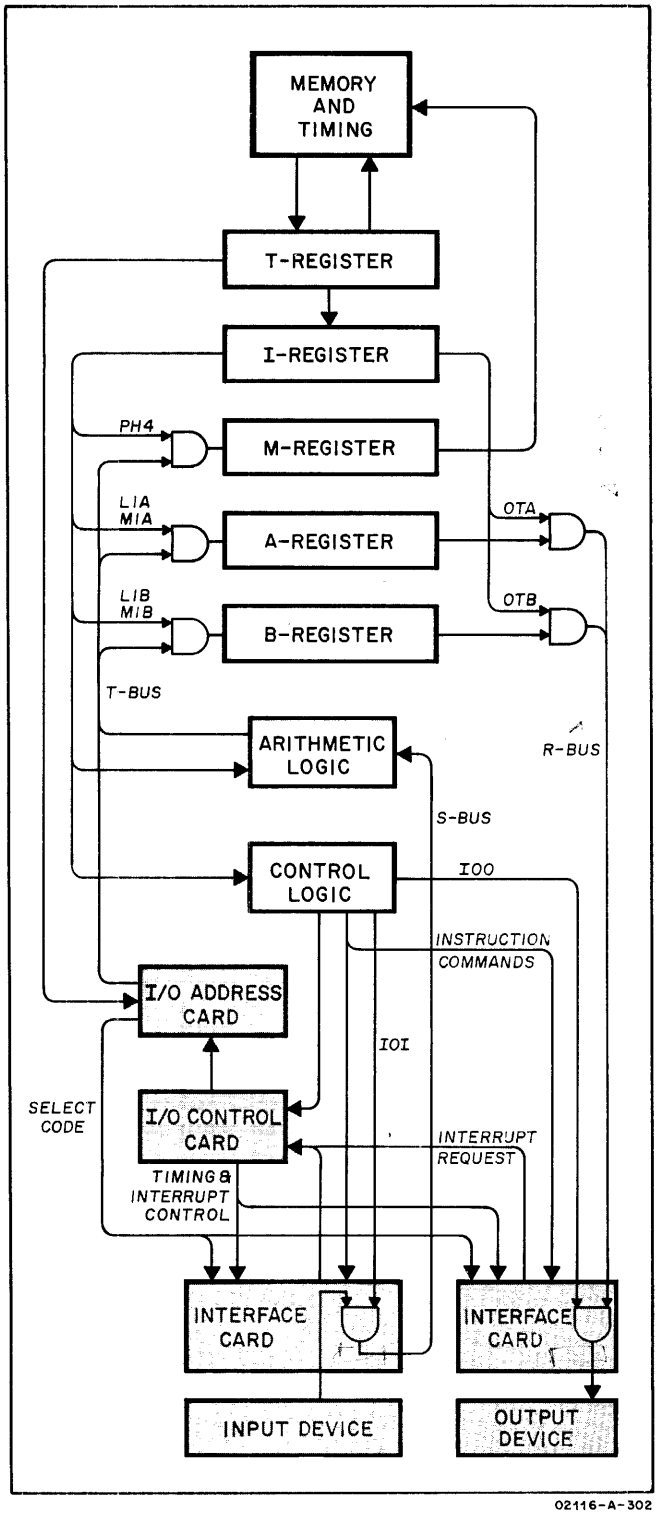


Figure 2-2. Block Diagram of System Input/Output Operations

2-11. Another driving signal from the Control Logic, the IOO (I/O Output) signal, strobes all interface cards to output data as a result of an OTA (Output from A) or an OTB (Output from B) instruction. The Select Code from the T-Register via the I/O Address card permits the IOO signal to strobe the data on the R-Bus into the appropriate interface card and external device. (The data was placed on the R-Bus from the A- or B-Register as a result of the OTA/B instruction.)

2-12. INTERRUPT REQUESTS

2-13. If a specific instruction to the I/O Control card has at some previous time enabled the interrupt system, an external device may request an interrupt to the computer program to obtain new data from the computer or to feed new data to the computer. This interrupt request is received by the I/O Control card. The I/O Control card signal to the I/O Address card causes it to interrupt the computer program by forcing the M-Register to be set (via the T-Bus) to a memory location corresponding to the Select Code of the interrupting device. This occurs during the interrupt phase 4 machine cycle. The Fetch phase is then entered to make the computer execute the instruction contained in the specified memory location. Generally, this instruction will be a jump to a service subroutine which will prepare or accept the new data. On completion of service, the subroutine must cause a return to the proper location in the main program. Refer to Paragraphs 2-28 through 2-53 for more detailed information on the interrupt system.

2-14. INPUT/OUTPUT SYSTEM CARDS

2-15. I/O CONTROL AND I/O ADDRESS CARDS

2-16. The computer contains one plug-in I/O Control card and one plug-in I/O Address card. The cards plug into the computer, adjacent to the interface cards as shown in Figure 2-3. Each card contains extractor handles to aid in their removal from the computer. Both cards are connected in parallel with all interface cards in the computer. The I/O Control Card contains the master Interrupt System Enable FF, receives command and timing signals from the computer for transfer to the interface card slots, and provides the necessary gates and flip-flops for proper control of interface-card operation. For detailed information on the I/O Control card, refer to Section III of this manual. The I/O Address card provides a decoding function for program selection of the desired interface card and an encoding function for interface card interrupt identification. For detailed information on the I/O Address card, refer to Section IV of this manual.

SELECT CODES				POSITION
			I/O CONTROL CARD	201
			I/O ADDRESS CARD	202
11	10		HIGH-SPEED PHOTO READER	203
12	11		HIGH-SPEED TAPE PUNCH	204
13	12		TELEPRINTER INPUT AND OUTPUT	205
14	13		PRIORITY JUMPER CARD	206
15	14			207
16	15			208
17	16			209
20	17			210
21	20			211
22	21			212
23	22			213
24	23			214
25	24			215
26	25			216
27	26			217
30	27		(RESISTANCE LOAD CARD)	218
-	-		I/O EXTENDER DRIVER	219
-	-		I/O EXTENDER DRIVER	220
-	-		MEMORY EXTENDER DRIVER	221
			MEMORY EXTENDER DRIVER	222

INTERFACE CARDS

LOWER SELECT CODE (HIGH PRIORITY)

HIGHER SELECT CODE (LOW PRIORITY)

Figure 2-3. Computer Plug-In Card Positions, Front View

2-17. RESISTANCE LOAD CARD

2-18. The computer contains one plug-in Resistance Load card. The card provides 17 150-ohm resistors, connected to the -2 volt supply, to load the termination of the IOBO (I/O Bus Output) lines from the computer to the interface cards. The card plugs into Position 218 (the last interface-card slot) of the Input/Output slots (Figure 2-3) of the computer. The card remains in slot position 218 unless the total interface and Priority Jumper cards used in the system equal 16. At that time, the card is no longer required and should be removed. Extractor handles on the card aid in its removal. Refer to Section V for further information on the Resistance Load card.

2-19. INTERFACE CARDS

2-20. PURPOSE. The interface cards provide channels through which data is transferred between the computer and the Input/Output devices, and provide control (via computer commands) of the Input/Output device operation. An interface card may contain up to 16 buffer FFs for temporary storage of data to be transferred to the computer or the Input/Output device. The number of buffer FFs on a particular interface card depends on the type of device connected to it. Other logic circuitry on the interface card also depends on the device to which it is connected. Certain devices are capable of interrupting the computer program while for others, this capability is not necessary; certain devices require control signals for movement of tape while others do not, etc., and timing requirements for some devices must be provided on the interface card. For detailed information on a particular interface card, refer to the applicable Interface Kit section of this manual. In some cases, more than one interface card is required for an external device; the interface cards necessary for the external devices are listed in Table 2-5 at the end of this section.

2-21. LOGIC ELEMENTS. Logic elements on the interface cards are provided by Microcircuit Packages which may contain more than one logic element and which are in numbered locations on the interface cards. The Microcircuit Package reference designations on the logic diagrams are preceded by MC. The number following MC corresponds to the numbered location of the package on the particular interface card. The individual elements of a package are further identified by a suffix letter. Figure A-1 in Appendix A provides logic diagrams for each of the Microcircuit Packages according to HP part number, the last three digits of which are stamped

on the Microcircuit Package. EXAMPLE: The reference designation MC67A refers to logic element A of the Microcircuit Package at location 67 on the interface card. The package will have a number stamped on it. If, for this example, the number 953 is stamped on the package, the logic diagram for the package is shown in Figure A-1 under the number 1820-0953. This diagram identifies element A as the "and" gate connected to pins 1, 2 and 14 of the Microcircuit Package.

2-22. PIN ASSIGNMENTS. Refer to Figure 2-4. One end of each interface card has 86 printed-circuit paths, 43 on each side of the card. This end of the card plugs into a computer slot connector to transfer signals to and from the computer. It is also keyed to prevent incorrect insertion. The circuit path positions correspond to the pin positions of the slot connector. Odd-numbered pins 1 through 85 are on one side of the card as shown in Figure 2-4, and even-numbered pins 2 through 86 are on the other side of the card. Pins 1 and 2 are directly opposite each other on the card. Pin assignments for this end of the card are identical for all interface cards to permit the placement of any card in any of the Input/Output slots of the computer.

2-23. The other end of the interface card has 48 printed-circuit paths, 24 on each side of the card. The plug connector of the interconnecting cable to the Input/Output device plugs into this end of the card to transfer signals to and from the device. The circuit-path positions correspond to the pin positions of the plug connector. Pins 1 through 24 are on one side of the card as shown in Figure 2-4, and consecutively-lettered pins A through BB (with letters G, I, O and Q missing) are on the other side of the card. Pins 1 and A are directly opposite each other on the card. Also on this end of the card are two extractor handles to aid in the removal of the card from the computer.

2-24. Refer to Table 2-1 for a list of the pin connections and signals between the interface cards and the slot connectors. Although this table lists all of the pin assignments and signals between the cards and the slot connectors, an individual interface card may not necessarily use all signals. Pin assignments and signals between an interface card and its Input/Output device is provided in each Interface Kit section of this manual.

2-25. INPUT/OUTPUT DEVICE SELECTION

2-26. Bits 0 through 5 of the Input/Output instruction form a Select Code to specify one of 64 possible Input/Output devices or functions. The Select Code is applied to the I/O Address card. This card decodes the 6-bit code and provides a two-digit octal code output. This output is transferred to the interface-card slot of the selected Input/Output device to

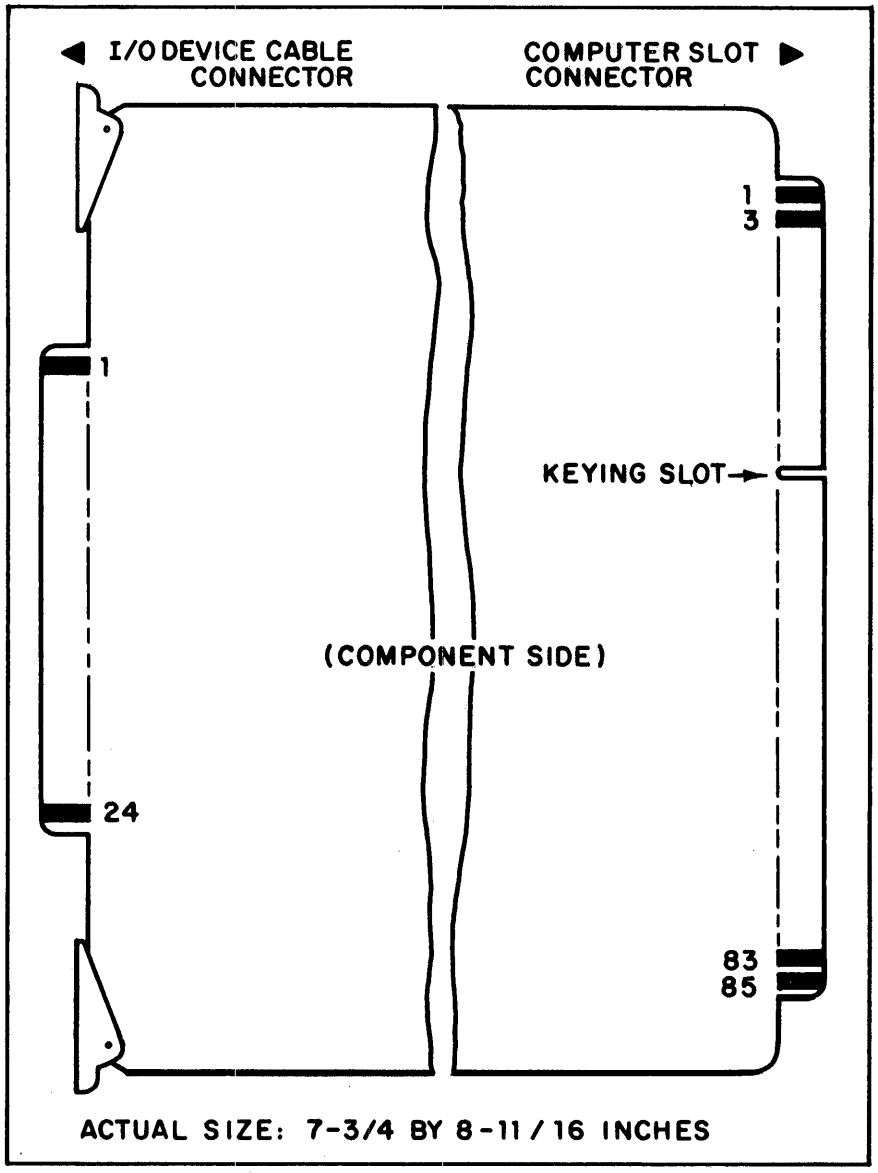


Figure 2-4. Interface Card Connectors

Table 2-1. Interface Card-to-Computer Pin Connections

PIN	SIGNAL	PIN	SIGNAL
1	Ground	2	Ground
3	PRL: Priority Low	4	FLGL: Flag signal, Lower Select Code
5	SFC: Skip Flag Clear (Skip next instruction if Flag FF is reset)	6	IRQL: Interrupt Request, Lower Select Code
7	CLF: Clear (reset) Flag FF	8	IEN: Interrupt Enable
9	STF: Set Flag FF	10	IAK: Interrupt Acknowledge
11	T3(B): Machine phase time T3 (Buffered)	12	SKF: Skip Flag (Skip next instruction if SFS or SFC test is true)
13	CRS: Control Reset	14	LSCM: Lower Select Code Most Significant Digit
15	IOG(B): I/O Group instruction (Buffered)	16	LSCL: Lower Select Code Least Significant Digit
17	POPIO(B): Power On Preset I/O (Buffered)	18	IOBI 16: I/O Bus Input, Bit 16
19	SRQ: Service Request	20	IOO: I/O Output
21	CLC: Clear (reset) Control FF	22	STC: Set Control FF
23	PRH: Priority High	24	IOI: I/O Input
25	SFS: Skip Flag Set (Skip next instruction if Flag FF is set)	26	IOBI 0: I/O Bus Input, Bit 0
27	IOBI 8: I/O Bus Input, Bit 8	28	IOBI 9: I/O Bus Input, Bit 9
29	IOBI 1: I/O Bus Input, Bit 1	30	IOBI 2: I/O Bus Input, Bit 2
31	IOBI 10: I/O Bus Input, Bit 10	32	SIR: Set Interrupt Request
33	IRQH: Interrupt Request, Higher Select Code	34	HSCL: Higher Select Code Least Significant Digit
35	IOBO 0: I/O Bus Output, Bit 0	36	+30 volts, unregulated
37	HSCM: Higher Select Code Most Significant Digit	38	IOBO 1: I/O Bus Output, Bit 1
39	+4.5 volts	40	+4.5 volts
41	IOBO 2: I/O Bus Output, Bit 2	42	IOBO 4: I/O Bus Output, Bit 4
43	+12 volts	44	+12 volts
45	IOBO 3: I/O Bus Output, Bit 3	46	ENF: Enable Flag
47	-2 volts	48	-2 volts
49	FLGH: Flag signal, Higher Select Code	50	(Not Used)
51	IOBO 5: I/O Bus Output, Bit 5	52	IOBO 7: I/O Bus Output, Bit 7
53	IOBO 6: I/O Bus Output, Bit 6	54	IOBO 8: I/O Bus Output, Bit 8
55	IOBO 11: I/O Bus Output, Bit 11	56	IOBO 9: I/O Bus Output, Bit 9
57	IOBO 12: I/O Bus Output, Bit 12	58	IOBO 10: I/O Bus Output, Bit 10
59	LDS: Load Switch	60	IOBI 11: I/O Bus Input, Bit 11
61	IOBO 13: I/O Bus Output, Bit 13	62	(Not Used)
63	(Not Used)	64	IOBI 3: I/O Bus Input, Bit 3
65	IOBO 14: I/O Bus Output, Bit 14	66	(Not Used)
67	(Not Used)	68	(Not Used)
69	-12 volts	70	-12 volts
71	(Not Used)	72	(Not Used)
73	IOBO 16: I/O Bus Output, Bit 16	74	IOBO 15: I/O Bus Output, Bit 15
75	(Not Used)	76	(Not Used)
77	IOBI 4: I/O Bus Input, Bit 4	78	IOBI 12: I/O Bus Input, Bit 12
79	IOBI 13: I/O Bus Input, Bit 13	80	IOBI 5: I/O Bus Input, Bit 5
81	IOBI 6: I/O Bus Input, Bit 6	82	IOBI 14: I/O Bus Input, Bit 14
83	IOBI 15: I/O Bus Input, Bit 15	84	IOBI 7: I/O Bus Input, Bit 7
85	Ground	86	Ground

NOTE: Pins 1&2, 39&40, 43&44, 47&48, 69&70, and 85&86 connected together on Slot Connector and on Interface Card.

permit program control of the device . Table 2-2 lists the Select Codes and their assignments, and indicates the corresponding interrupt location (i. e., the memory location containing the instruction to be executed when an interrupt occurs). Select Code 00 is the access to the master Interrupt System Enable FF on the I/O Control card. Codes 01 through 06 are reserved for processor Input/Output functions or options, as listed. Codes 10 through 76 (octal) are used for selection of the 55 possible Input/Output devices, each capable of causing an interrupt. The last Select Code, 77, is reserved for an interrupt caused by a program attempt to alter the contents of a memory location protected by Memory Protect Option M1.

2-27. Figure 2-3 illustrates the slots in the computer for the plug-in cards associated with Input/Output operation. Each of the interface-card slots actually has two Select Codes assigned to it. This provides for interface cards which contain both input and output logic circuits (e. g., Teleprinter Input and Output in Position 205 of Figure 2-3). The input portion and the output portion of the card each require a separate Select Code. When an interface card contains addressable input and output logic, the adjacent slot (Position 206 in Figure 2-3) cannot contain another addressable interface card. Instead, a Priority Jumper card must be inserted in the slot to maintain priority continuity as described in Paragraph 2-45. Since the slot connector wiring determines the Select Codes of the slots and interface cards can be plugged into any slot, the interface card assumes the Select Codes of the slot it is plugged into. (Interface cards are assigned to particular slot positions before shipment of a computer system and may vary from system to system. The slot positions of the interface cards in Figure 2-3 are for illustration purposes only.)

2-28. INTERRUPT SYSTEM

2-29. The Interrupt System provides the means for an external device to interrupt the program in progress when data is available or when additional output data can be accepted. Figure 2-5 illustrates the relationship between the computer, the I/O Control and I/O Address plug-in cards, and typical interrupt logic on a particular interface card; Figure 2-5 is for interrupt-logic explanatory purposes only. Refer to Figure 2-6 for a chart of typical interrupt system timing.

2-30. An interrupt request from an external device occurs when the following conditions are met:

a. The Interrupt System is enabled.

b. The Flag FF of the specific device interface card is set.

Table 2-2. Select Code Assignments

SELECT CODE (OCTAL)	INTERRUPT LOCATION	ASSIGNMENT
00	None	Interrupt System Disable/Enable
01	None	Switch Register or Overflow
02	None	DMA Channel 1 Initialize
03	None	DMA Channel 2 Initialize
04	None	(Not Assigned)
05	00005	Power Failure Interrupt
06	00006	DMA Channel 1 Completion Interrupt
07	00007	DMA Channel 2 Completion Interrupt
10	00010	I/O Device, Highest Priority
thru	thru	thru
76	00076	I/O Device, Lowest Priority
77	00077	Memory Protect Interrupt

c. The Control FF of the specific device interface card is set.

d. No priority-effecting instruction (STF, CLF, STC and CLC) is in progress.

e. No higher-priority devices satisfy the conditions of steps "a" through "d".

2-31. INTERRUPT SYSTEM ENABLE-DISABLE

2-32. The computer program determines if interrupt requests from the external devices will be recognized. This is accomplished by enabling or disabling the Interrupt System Enable FF on the I/O Control card. A Set Flag (STF) instruction with a Select Code of 00 (octal) sets the FF and enables the interrupt system. A Clear Flag (CLF) instruction with a Select Code of 00 (octal) resets the FF and disables the interrupt system.

2-33. When computer power is initially turned on, pressing the POWER pushbutton automatically resets the Interrupt System Enable FF, disabling the interrupt system. Initial turn-on also resets all Control FFs on the interface cards to prevent Input/Output devices from running when power is applied, and sets all Flag Buffer and Flag FFs on the interface cards. Therefore, to operate any device, it is first necessary to set the Interrupt System Enable FF, reset the individual Flag Buffer and Flag FFs, and set the individual Control FF.

2-34. INTERRUPT SYSTEM OPERATION

2-35. When the external device has completed its operation, it generates a Device Flag signal to the Interface-card Flag Generator which sets the Flag Buffer FF (see Figure 2-5). The output of the Flag Buffer FF, in conjunction with the ENF (Enable Flag) signal from the I/O Control card at time T2 (Figure 2-6) causes "and" gate A to set the Flag FF. The Flag FF output is "anded" at gate B with the output of "and" gate C. The gate C output is true when the Control FF is set and when the IEN (Interrupt Enable) signal is received from the I/O Control card at time T3. Unless the Control FF is set by a Set Control (STC) instruction, an interrupt request cannot occur.

2-36. The Control FF is set under program control and therefore, may be set at any T4 time of a machine cycle, depending on the type of operation being performed. The STC instruction is enabled to the Control FF by the SCM (Select Code Most significant digit) and SCL (Select Code Least

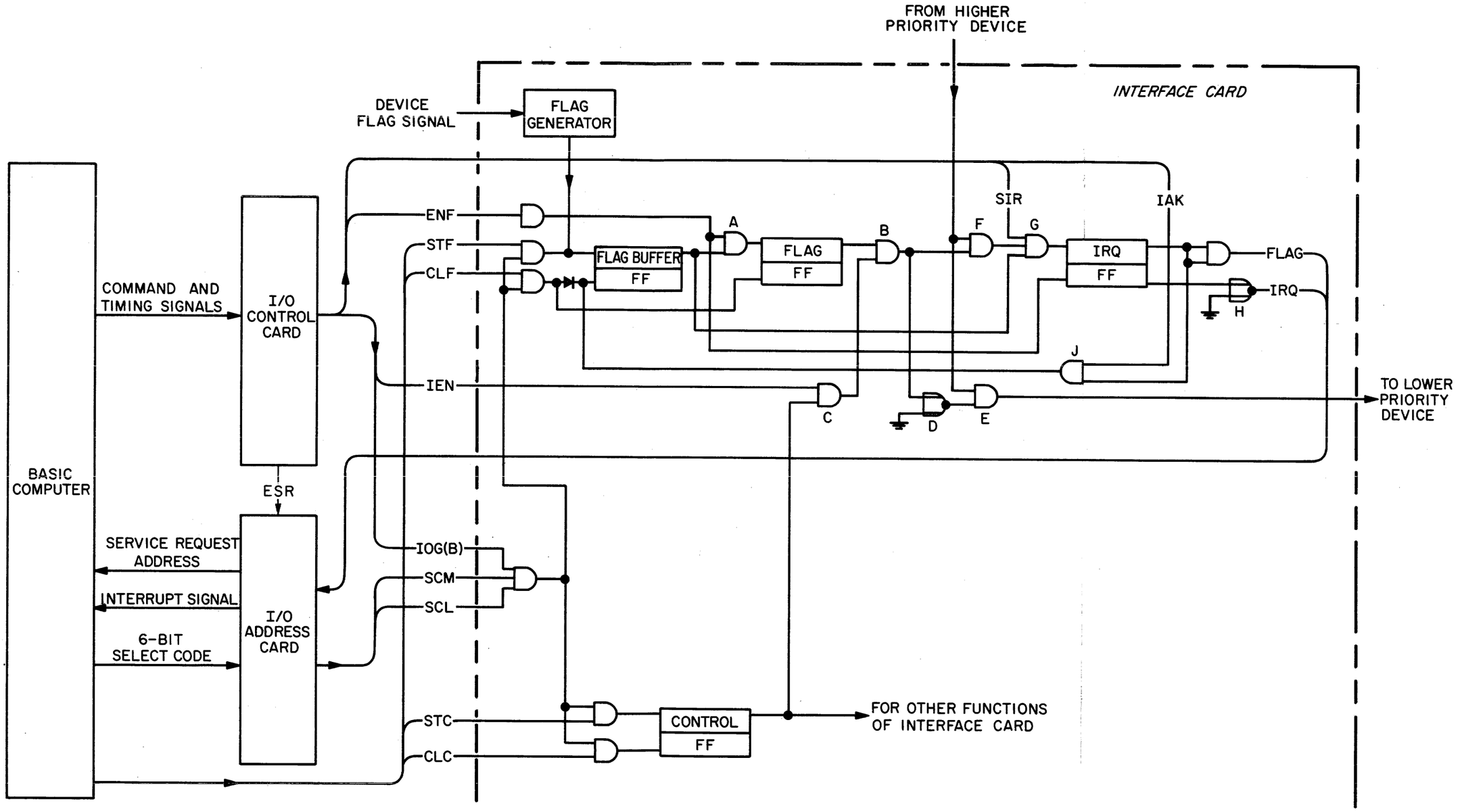
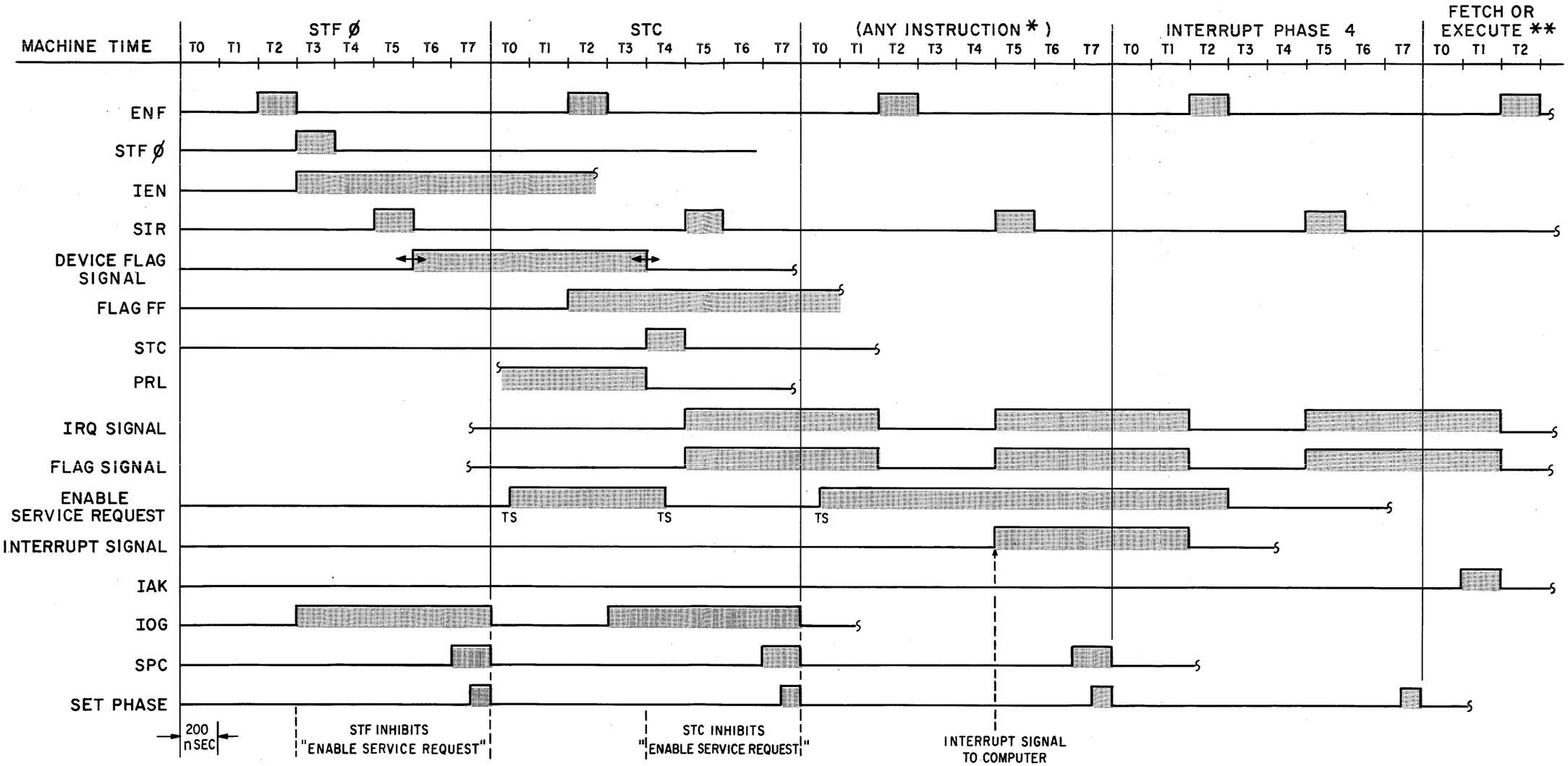


Figure 2-5. Typical Interrupt Logic



NOTES:

* EXCEPT STF, CLF, STC, CLC, JMP I, AND JSB I.
** EXECUTE IF A SINGLE CYCLE INSTRUCTION.

Figure 2-6. Typical Interrupt System Timing

significant digit) signals from the I/O Address card, and the IOG (B) (I/O Group instruction, Buffered) signal from the I/O Control card. The SCM and SCL signals are enabled on the individual interface card by the IOG(B) signal which occurs when the instruction to be performed is an I/O Group instruction. When the Control FF sets, a true input is applied to "and" gate C. The inputs to "and" gates B and C are then true and gate B applies a true output to inverting "or" gate D. The false output of gate D disables "and" gate E, making the priority network bus to the lower-priority devices false. This prevents any device of lower priority from requesting an interrupt.

2-37. At the same time that gate B applied a true output to gate D, it also applied a true output to "and" gate F. The priority network signal to gate F will be true if an interface card (device) of higher priority than the one represented in Figure 2-5 is not requesting an interrupt. In this case, the true output of gate F is combined with the SIR (Set Interrupt Request) signal from the I/O Control card at time T5 and the output of the set Flag Buffer FF to provide a true output from "and" gate G. The gate G output sets the IRQ (Interrupt Request) FF.

2-38. The IRQ FF outputs provide the Flag signal and the IRQ signal to the I/O Address card. (The IRQ signal is obtained by the inversion of the false reset-side output of the IRQ FF by inverting "or" gate H.) The Flag signal is "anded" in the I/O Address card with the Enable Service Request (ESR) signal from the I/O Control card to form an interrupt signal. However, the ESR signal is false for the remainder of the machine cycle during which an instruction occurs that effects device priorities (STC in Figure 2-6) as determined by the I/O Control card. At time T2, the IRQ FF is reset by the ENF signal to allow a higher-priority device to request an interrupt. If the Control FF is still set and no higher-priority devices have requested an interrupt, the IRQ FF will again be set at time T5 (SIR). The Flag and IRQ signals are again sent to the I/O Address card. The signals are used to form a 6-bit Service Request Address to be enabled to the computer at time T7 of Interrupt Phase 4. The Flag signal and the now-true ESR signal form the Interrupt signal which is sent to the computer. This signal causes an interrupt at the end of the current machine phase, switching the computer into the Interrupt Phase except when any of the following conditions occur:

a. The computer is in the HALT mode.

b. A Jump Indirect (JMP,I) or a Jump to Subroutine Indirect (JSB,I) instruction is not fully executed. (These instructions inhibit all interrupts until fully executed for any number of indirect levels of addressing. At the earliest, an interrupt request will be granted at the end of the machine phase immediately following one or more JMP,I or JSB,I instructions.)

c. A Direct Memory Access (DMA) option is in process of transferring data. Exception: The Power Failure Control Option M8 can interrupt a DMA transfer.

2-39. INTERRUPT PROCESSING

2-40. During Interrupt Phase 4, the computer decrements the P-register by one to ensure that the proper location in the main program will be returned to after the interrupt is processed. (The P-register was incremented by one at time T7 of the last machine phase of the main program by the SPC (Step Program Counter) signal.) Also, the computer places the Service Request Address (which is always equal to the Select Code of the interrupting device) from the I/O Address card into the M-register at time T7. This causes the next instruction to be read from the memory location having the same number as the Service Request Address (Select Code) during the Fetch Phase (Phase 1). This location in memory is referred to as the "interrupt location" and is reserved for that particular device. Example: A device specified by a Select Code of 10 will interrupt to (i. e., cause execution of the contents of) memory location 00010. At time T3 of Phase 4, the interrupt system is inhibited by the false Enable Service Request signal until the Fetch Phase following the execution of the instruction at the interrupt location. This prevents interrupts from occurring until at least one instruction has been executed (except in the case of JMP,I and JSB,I instructions).

2-41. At time T1 of Fetch Phase 1 the IAK (Interrupt Acknowledge) signal from the I/O Control card and the set-side output of the IRQ FF resets the Flag Buffer FF through "and" gate J (Figure 2-5). Since the set-side output of the Flag Buffer FF is applied to "and" gate G, resetting the FF prevents the setting of the IRQ FF and causing another interrupt from the same Flag signal at time T5 of Phase 1 when the SIR signal is again applied to gate G. (The Flag Buffer FF can also be reset by a programmed CLF (Clear Flag) instruction.) At time T2, the ENF signal resets the IRQ FF. The computer fetches the instruction in the interrupt location which will usually be a jump to a subroutine (JSB,I) instruction, although any legal instruction may be placed in the interrupt location. The contents of the P-register plus one is stored in the first location (X) of the subroutine. (Since the previous contents of the first memory location are destroyed when P+1 is stored, the first instruction of the subroutine should always be a no-operation (NOP) instruction or equivalent.) The location of the subroutine (X+1) is placed in the P- and M-registers, and the computer resumes normal subroutine operation. Thus, the instruction at location X+1 is the first instruction of the subroutine to be executed. The contents of the working registers that were in use in the main program should be stored when entering the subroutine and restored before exit from the

subroutine. The exit from the subroutine is made with a JMP,I to location X. This places the address of the interrupted program instruction in the P- and M-registers and normal program operation resumes.

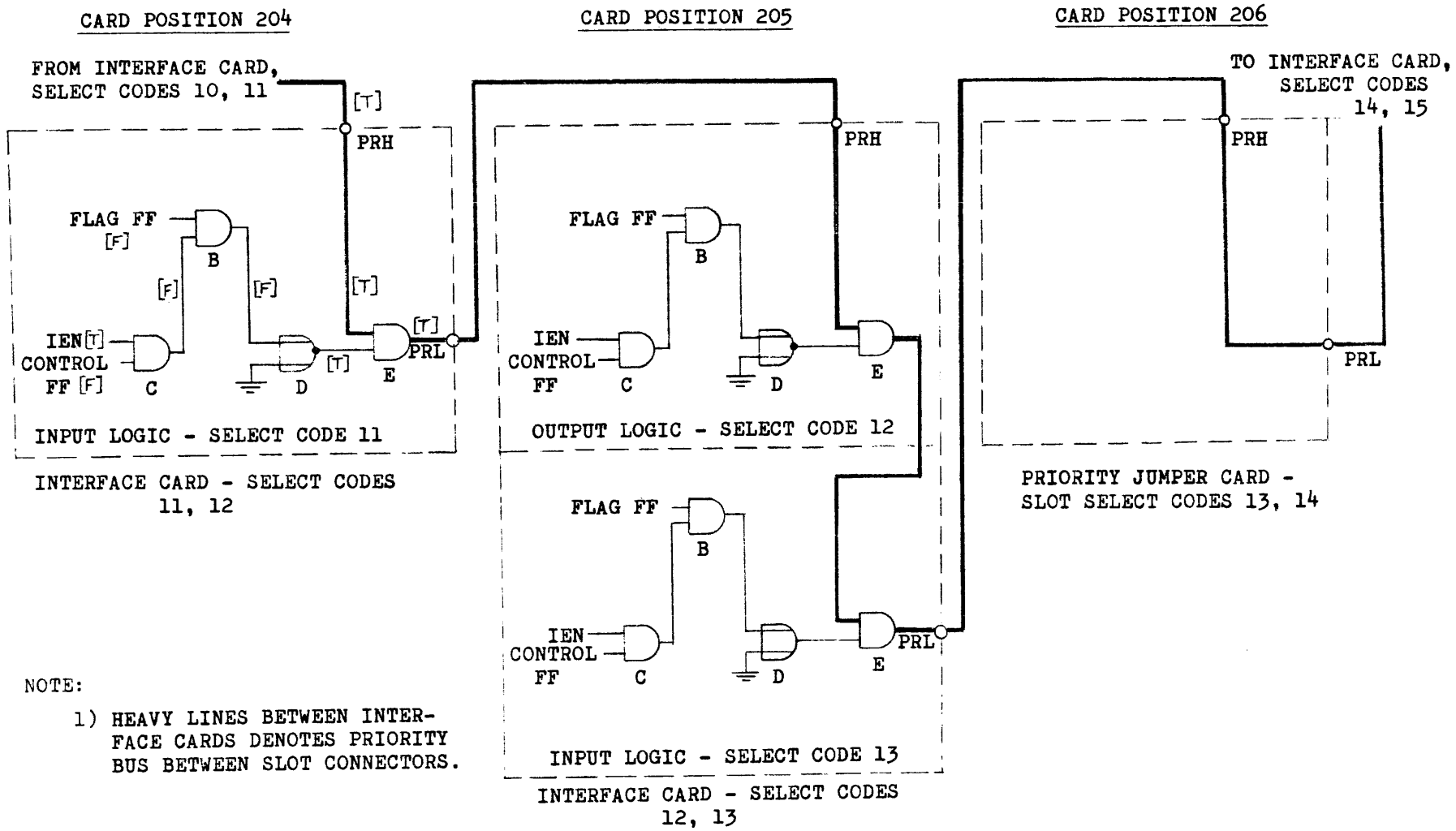
2-42. INTERRUPT PRIORITY

2-43. PRIORITY ASSIGNMENTS. A priority network on the interface cards allows only one external device to interrupt the computer program regardless of the number of devices requesting an interrupt. The priority network gives highest priority to Select Code 05, reserved for Power Failure Control Option M8, and decreasing priority to Select Codes in order from 06 through 77 (see Table 2-2). The transfer of data by the two optional Direct Memory Access (DMA) channels effectively have priorities between Select Codes 05 and 06, since they can inhibit all interrupts except Power Failure Control. DMA Channel 1 has priority over DMA Channel 2.

2-44. As shown in Figure 2-3, each of the interface-card slots in the computer is assigned two interrupt priorities corresponding to the two Select Codes assigned each slot. This provides an interrupt priority for both the input and output portions of an interface card. The interrupt priority assignments of each slot remain fixed but since any interface card can be plugged into any slot, the interrupt priority of a given device can be easily changed by plugging the device interface card into another slot.

2-45. PRIORITY NETWORK OPERATION. As shown in Figure 2-7, priority is established by a hardware-implemented priority chain. The "and-or" gates illustrated in Figure 2-7 are identified by letters and correspond to those used in Figure 2-5. The true-false logic levels for an interface card which is not requesting an interrupt are illustrated on the first interface card (Select Codes 11, 12) with the Interrupt System enabled (IEN input is true). Also, the PRH (Priority High) signal is true, indicating that a device of higher priority is not requesting an interrupt. In this case, the "chain" is not broken and a true PRL (Priority Low) signal is available to the next interface card (Select Codes 12, 13) as a true PRH signal to that card.

2-46. The interface card with Select Codes of 12 and 13 in Figure 2-7 contains both input and output logic. Each type of logic has a separate Select Code and corresponding interrupt priority, with the priority chain connected internally. The output logic of the interface card is always of higher priority than the input logic on cards containing both types of logic. Since this interface card uses both Select Codes assigned to its slot, an



NOTE:

1) HEAVY LINES BETWEEN INTERFACE CARDS DENOTES PRIORITY BUS BETWEEN SLOT CONNECTORS.

Figure 2-7. Interrupt Priority

addressable interface card cannot be placed in the adjacent slot (Card Position 206). However, the adjacent slot must contain a Priority Jumper card to provide continuity for the priority network. There can be no gaps in the network for it to function properly. This card is shown in Card Position 206 of Figure 2-7.

2-47. If the output logic portion of the interface card with Select Codes of 12 and 13 in Figure 2-7 requests an interrupt, all inputs to "and" gate B will be true. Inverting "or" gate D will then apply a false input to "and" gate E. The output of gate E is then false, breaking the "chain", and preventing any interface card of lower priority from interrupting the computer program. A service subroutine can then be entered to process the interrupt of the output logic.

2-48. A service subroutine of any device can be interrupted by a higher-priority device; then after the higher-priority interrupt subroutine is completed, the lower-priority subroutine may continued. In this way, several service subroutines may be in a state of interruption at one time. Each will be permitted to continue when the next higher priority subroutine is completed.

2-49. Interrupt priority can also be program controlled. Since an interrupt cannot occur unless the Control FF of the interface card is set, all Control FFs on interface cards of higher priority than the one desired can be reset by a Clear Control (CLC) instruction. This prevents those interface cards from requesting an interrupt and establishes the desired device as the highest-priority device.

2-50. INTERRUPT PRIORITY CONTINUITY

2-51. Figure 2-8 illustrates the continuity of the interrupt priority network for all possible Input/Output interface cards and processor option cards capable of interrupting the computer. The Interrupt System Enable FF and gates A, B, and C shown in Figure 2-8 are located on the I/O Control card. Gates D through I are contained in their respective Extender Module.

2-52. Since the Power Failure Control option (Select Code 05) is assigned the highest priority, it can interrupt the computer regardless of the state of the Interrupt System Enable FF. For all other interface cards and options, the FF must be set before an interrupt can occur. When an interface card requests an interrupt, its false PRL signal is applied to the next interface card as a false PRH signal to prevent it from requesting an interrupt. This sequence continues from card to card until the last interface card receives a false PRH signal. If a

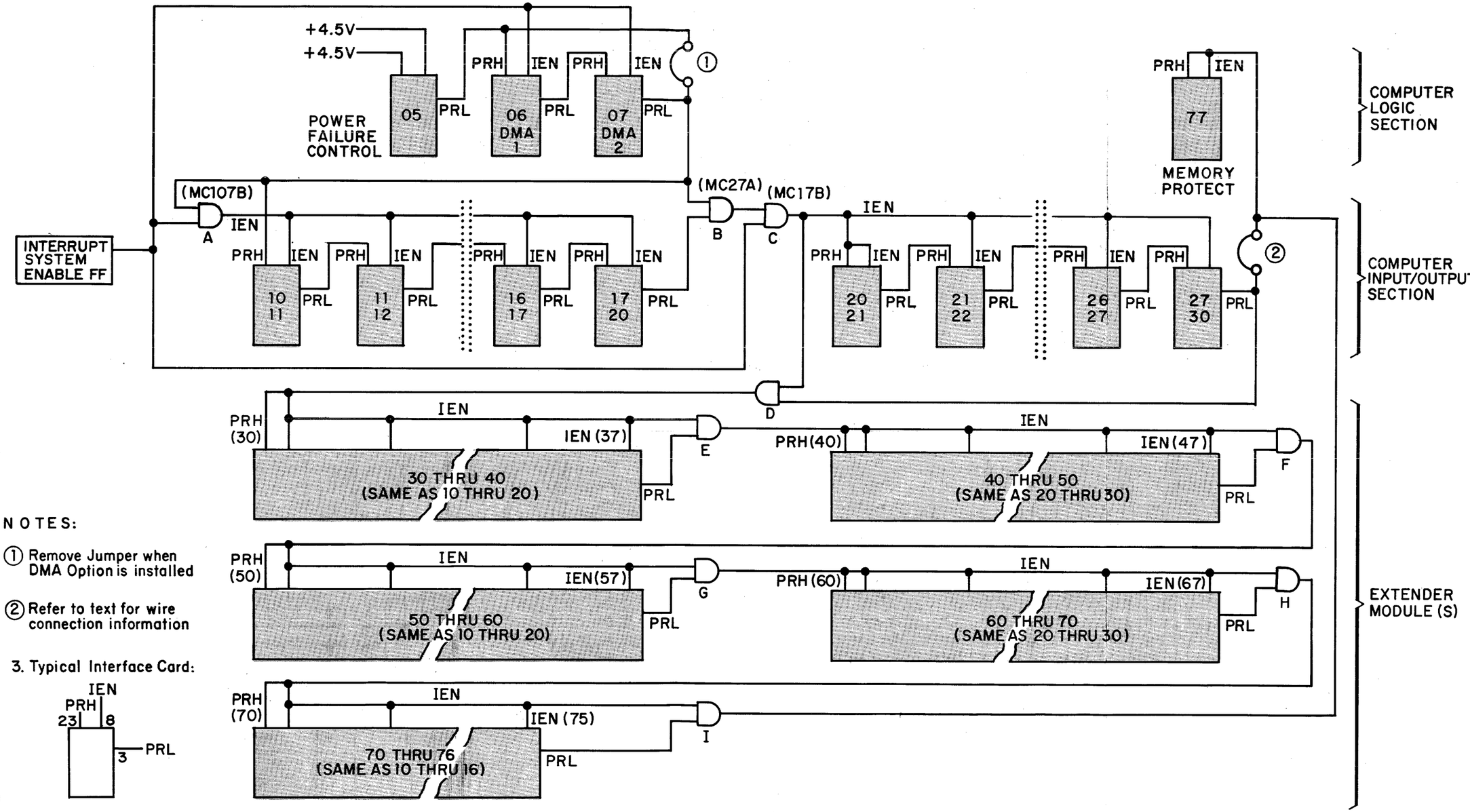


Figure 2-8. Interrupt Priority Continuity

large number of interface cards are used in the system and a card of high priority requests an interrupt, the switching times required by the cards may cause a delay sufficient to enable a card of low priority to interrupt before its PRH signal input becomes false, causing dual interrupt requests. To prevent this condition from occurring, "and" gates are provided for each set of eight cards in parallel and therefore can disable all eight cards simultaneously. Thus, when an interrupt request occurs, the PRL-PRH switching sequence proceeds to the "and" gate following the group of eight cards in which the interrupt request occurs. The false input to the "and" gate causes a false IEN output and all following interface cards are immediately disabled.

2-53. When the Memory Protect option, Select Code 77, is installed in the computer, it should be connected such that it follows the last interface card used. When only the 16 interface cards in the basic computer are used, it should be connected to the PRL output of the interface card with Select Codes of 27 and 30 via the jumper indicated in Figure 2-8. When additional interface cards are added through the use of an Extender Module, the Memory Protect option should be connected to the output of the "and" gate following the last group of eight cards added. If less than an entire group of eight interface cards are added, Priority Jumper cards should be inserted to fill-out the group. When the maximum number of interface cards (Select Codes 10 through 76) are used, the option should be connected as shown in Figure 2-8, except that the jumper on the PRL output of the interface card with Select Codes of 27 and 30 should be removed.

2-54. EXTENDER MODULE

2-55. An HP 2150A Extender Module must be used when more than 16 interface cards are required for the computer system. The extender module is a separate rack-mount unit which is similar in physical dimensions and internal construction to the basic computer. It contains its own power supply. Since the basic computer control logic will not be present in the extender module, all three plug-in card sections are available for expanding the memory and Input/Output capabilities. Up to 32 interface cards may be plugged into the extender module. (With the 16 interface cards plugged into the basic computer, the extender module extends the total interface-card capability of the computer system to 48 interface cards.) However, the extender module alone is incomplete and requires one or more of the following extender-module Options to complete its extension facility. Options M1 and M2 are available only with the initial extender module order; Option M3 can be added at any time.

a. Option M1: This option comprises four plug-in cards which are required for the operation of the interface cards (up to 32) added to the extender module.

b. Option M2: This option comprises a set of plug-in memory addressing cards, two integral connecting cables, and a 4K (4,096 words) memory module. This Option, combined with the 8K memory in the basic computer, gives a total memory size of 12K (12,288 words).

c. Option M3: This option comprises a set of plug-in memory addressing cards and a 4K memory module to add a second 4K memory to an extender module containing Option M2 (HP 2150A-M2). This Option, combined with the 8K memory in the basic computer and the 4K memory of Option M2, gives a total memory size of 16K (16,384 words).

2-56. POWER SUPPLY REQUIREMENTS

2-57. The computer internal power supply is adequate for a full complement of plug-in options (16) if all the options have low-current requirements. External power from an HP 2160A Power Supply may be required if certain options with high-current requirements are plugged into the computer. Both power supplies provide voltages of +12, -12, -2, and +4.5 volts. The 2160A Power Supply can be mounted in a standard 19-inch rack and is connected to the computer power supply, for computer control, by a single cable.

2-58. Table 2-3 lists the current available from the computer power supply and from the combination of computer power supply and 2160A Power Supply. The current available for options in Table 2-3 is obtained by subtracting the current required by the computer from the current available from the power supplies. Table 2-4 lists the current required by the processor and Input/Output options. To determine if the computer power supply is adequate for the options to be used with the computer or if a 2160A Power Supply must be added, proceed as follows:

a. Refer to Table 2-4 and add the currents required in each of the +12V, -12V, -2V, and +4.5V columns for the selected options.

b. Add the sum of the -2V supply currents obtained in step "a" to the value in the +4.5V column of Table 2-3 for a computer with a 4K or 8K memory (as applicable) under the CURRENT AVAILABLE FOR OPTIONS title. Record this new sum.

Table 2-3. Internal/External Power Supply Requirements

REQUIREMENTS	SUPPLY CURRENTS (AMP)			
	+12V	-12V	-2V	+4.5V
CURRENT AVAILABLE FROM POWER SUPPLIES				
Computer Power Supply	3	3	22.5	*22.5
Computer & 2160A Power Supplies	3	3	32.5	**32.5
CURRENT REQUIRED BY COMPUTER WITH NO PROCESSOR OR INPUT/OUTPUT OPTIONS				
Computer with 4K Memory	0.05	0.6	13.5	24.0
Computer with 8K Memory	0.05	1	14.0	28.0
CURRENT AVAILABLE FOR OPTIONS				
Computer with 4K Memory	2.95	2.4	9.0	***12.0
Computer with 8K Memory	2.95	2.0	8.5	*** 8.5
Computer with 4K Memory & 2160A Power Supply	2.95	2.4	19.0	***22.5
Computer with 8K Memory & 2160A Power Supply	2.95	2.0	18.5	***18.5

NOTES:

* Plus the current drawn from the -2V supply by the computer with memory and options. Maximum available from +4.5V supply is 45 amperes.

** Plus the current drawn from the -2V supply by the computer with memory and options. Maximum available from +4.5V supply is 65 amperes.

*** Plus the current drawn from the -2V supply by the selected options.

Table 2-4. Current Required by Options

OPTIONS	SUPPLY CURRENT REQUIRED (AMP)			
	+12V	-12V	-2V	+4.5V
PROCESSOR OPTIONS:				
M2 Memory Parity Check	0	0	0.5	0.53
M3 Memory Test	0	0.05	0.48	0.91
INPUT/OUTPUT OPTIONS:				
Teleprinter Input/Output	0.11	0.05	0.9	1.4
High-Speed Punched Tape Input	0.03	0.01	0.48	1.1
Digital Voltmeter Program Output (2401C)	0	0.3	0.24	0.42
Digital Voltmeter Program Output (3460A)	0	0.06	0.3	0.42
Crossbar Scanner Program Output	0.01	0.04	0.84	1.1
High-Speed Punched Tape Output	0.01	0.01	0.3	0.72
Incremental Magnetic Tape Output	0	0.06	0.48	0.9
Magnetic Tape Input/Output	0.09	0.18	4.2	6.6
Time Base Generator	0.01	0	0.42	1.1
Data-Phone Interface	0.11	0.05	0.9	1.4
Digital Voltmeter Data Input (2401C, 3440A, 3460A)	0.05	0.01	0.3	0.96
Counter/Thermometer Data Input (8 Digits)	0.05	0.01	0.3	0.96
Counter Data Input (4, 5, 6 & 7 Digits)	0.05	0.01	0.3	0.96
General Purpose Register	0.24	0.01	0.48	2.4

c. Again refer to the currents listed for a computer with 4K or 8K of memory (as applicable) under the CURRENT AVAILABLE FOR OPTIONS title in Table 2-3. If any of the individual +12V, -12V, or -2V supply current sums of step "a" are higher than those listed, or if the +4.5V supply current sum is higher than that recorded in step "b", a 2160A Power Supply is required. The current sums cannot then exceed those listed for a computer with a 4K or 8K memory (as applicable) and a 2160A Power Supply. If any are exceeded, a second 2160A Power Supply is required.

2-59. INTERFACE KITS

2-60. Interface Kits for the HP 2116A Computer System provide the necessary interface cards, priority jumper cards, and cables for connection of external equipment to the computer. The necessary software for driving the specific peripheral device, and the device diagnostic-program tape are also provided. The kits are identified by a 5-digit accessory number, a suffix revision letter, and a functional name (e.g., 12531A Teleprinter Input/Output). Table 2-5 lists the available interface kits, their hardware contents, and the external equipment which can be connected to the interface card or cards in the kit. Table 2-6 lists interface kits and the accessory numbers and names of the software binary tapes they contain. The tapes are identified by their name and HP accessory number on both the tape container and the tape itself. The tapes are also listed in the HP 2116A Software Catalog (a supplement to the HP 2116A Computer Technical Data sheet) and new additions will be added to the Catalog as they become available. Table 2-6 will be updated by revision of this manual.

Table 2-5. Input/Output Interface Kits

INTERFACE KIT NO. AND FUNCTION	FOR USE WITH THIS PERIPHERAL DEVICE (NOT INCLUDED IN KIT)	INTERFACE KIT INCLUDES		
		INPUT/OUTPUT CARDS	CARD PART NO. (02116-XXXX)	CABLE PART NO. (02116-XXXX)
12531A Teleprinter Input/Output	HP 2752A Teleprinter (Modified Teletype ASR33) HP 2754A Teleprinter (Modified Teletype ASR35)	Teleprinter Interface Card Priority Jumper Card	-6007 -6110	(Integral with Peripheral Device)
12532A High-Speed Punched Tape Input	HP 2737A Punched Tape Reader HP 2737B Punched Tape Reader-Spooler	Punched Tape Reader Interface Card	-6002	-6112
12533A Digital Voltmeter Program Output (HP 2401C)	HP 2401C Integrating Digital Voltmeter	Digital Voltmeter (Programmer) Interface Card	-6046	-6115
12534A Digital Voltmeter Program Output (HP 3460A)	HP 3460A Digital Voltmeter	Digital Voltmeter (Programmer) Interface Card	-6046	-6116
12535A Crossbar Scanner Program Output	HP 2911 Guarded Crossbar Scanner	Crossbar Scanner Interface Card	-6123	-6117 and 5060-2504
12536A High-Speed Punched Tape Output	HP 2753A Tape Punch	Tape Punch Interface Card	-6045	-6118

Table 2-5. Input/Output Interface Kits (Cont'd)

INTERFACE KIT NO. AND FUNCTION	FOR USE WITH THIS PERIPHERAL DEVICE (NOT INCLUDED IN KIT)	INTERFACE KIT INCLUDES		
		INPUT/OUTPUT CARDS	CARD PART NO. (02116-XXXX)	CABLE PART NO. (02116-XXXX)
12537A Incremental Magnetic Tape Output	Kennedy 1406 & 1506 Incremental Magnetic Tape Transports	Incremental Tape Transport Interface Card	-6128	-6147
12538A Magnetic Tape Input/ Output	HP H26-2020A Magnetic Tape Unit (200 bpi) HP H26-2020B Magnetic Tape Unit (200 & 556 bpi)	Magnetic Tape (Timing) Interface card	-6157	-6162
		Magnetic Tape (Control) Interface Card	-6158	-6161
12539A Time Base Generator	---	Time Base Generator Card	-6119	---
12540A Data-Phone Interface	Bell System Data Set 103A	Teleprinter Interface Card	-6007	-6156
		Priority Jumper Card	-6110	
12541A Digital Voltmeter Data Input (HP 2401C)	HP 2401C Integrating Digital Voltmeter	Data Source Interface Card	-6004	-6113
12542A Digital Voltmeter Data Input (HP 3460A)	HP 3460A Digital Voltmeter	Data Source Interface Card	-6004	-6114

Table 2-5. Input/Output Interface Kits (Cont'd)

INTERFACE KIT NO. AND FUNCTION	FOR USE WITH THIS PERIPHERAL DEVICE (NOT INCLUDED IN KIT)	INTERFACE KIT INCLUDES		
		INPUT/OUTPUT CARDS	CARD PART NO. (02116-XXXX)	CABLE PART NO. (02116-XXXX)
12543A Digital Voltmeter Data Input (HP 3440A)	HP 3440A Digital Voltmeter	Data Source Interface Card	-6004	-6154
12544A Counter/Thermometer Data Input (8 Digits)	HP 5245L Electronic Counter HP 2801A Quartz Thermometer	Data Source Interface Card	-6004	-6153
12545A Counter Data Input (7 Digits)	HP 5244L & 5275A Electronic Counters	Data Source Interface Card	-6004	-6163
12546A Counter Data Input (6 Digits)	HP 5201L, 5202L, 5203L, 5232A, 5233L and 5532A Electronic Counters	Data Source Interface Card	-6004	-6164
12547A Counter Data Input (5 Digits)	HP 5212L, 5214L, 5223L, and 5512A Electronic Counters	Data Source Interface Card	-6004	-6165
12548A Counter Data Input (4 Digits)	HP 5211A/B Electronic Counters	Data Source Interface Card	-6004	-6166

Table 2-5. Input/Output Interface Kits (Cont'd)

INTERFACE KIT NO. AND FUNCTION	FOR USE WITH THIS PERIPHERAL DEVICE (NOT INCLUDED IN KIT)	INTERFACE KIT INCLUDES		
		INPUT/OUTPUT CARDS	CARD PART NO. (02116-XXXX)	CABLE PART NO. (02116-XXXX)
12549A General Purpose Register	---	General Purpose Register Card	-6006	(Connector Kit) -6178
12550A Digital Voltmeter Program Output	HP 2401C Integrating Digital Voltmeter and HP 2411A Guarded Data Amplifier combination	Digital Voltmeter (Programmer) Interface Card	-6046	-6173

Table 2-6. Input/Output Interface Kit Software

INTERFACE KIT AND TAPES	HP ACCESSORY NUMBER
12531A INTERFACE KIT TELEPRINTER INPUT/OUTPUT	
BCS Teleprinter Driver	20004A
SIO 4K Teleprinter Driver, or	20302A
SIO 8K Teleprinter Driver (Option M4)	20305A
Teleprinter Test	20407A
12532A INTERFACE KIT HIGH-SPEED PUNCHED TAPE INPUT	
BCS Tape Reader Driver	20005A
SIO 4K Tape Reader Driver, or	20303A
SIO 8K Tape Reader Driver (Option M4)	20306A
Tape Reader Test	20408A
12536A INTERFACE KIT HIGH-SPEED PUNCHED TAPE OUTPUT	
BCS Tape Punch Driver	20006A
SIO 4K Tape Punch Driver, or	20304A
SIO 8K Tape Punch Driver (Option M4)	20307A
Tape Punch Test	20409A
12537A INTERFACE KIT INCREMENTAL MAGNETIC TAPE OUTPUT	
BCS Incremental Magnetic Tape Driver	20007A

SECTION III

I/O CONTROL CARD

3-1. INTRODUCTION

3-2. This section provides theory of operation information for the I/O Control card (HP Part No. 02116-6041). The card is of standard interface-card size and plugs into Position 201 on the left side of the Input/Output slots of the computer. The slot connector transfers signals to and from the card; no additional cabling is required. The card output signals are transferred to all interface cards in the computer, in parallel, through the interface-card slot connectors. The main function of the I/O Control card is to control the interrupt system. Certain clock signals, reset signals, and selection of the Switch and Overflow Registers of the computer is also provided by the I/O Control card.

3-3. THEORY OF OPERATION

3-4. COMPUTER POWER-ON

3-5. When power is initially applied by pressing the POWER push switch on the front panel of the computer, the computer is preset to time T5 of the Fetch Phase (Phase 1) At this time, the POPIO signal (Figure 3-2) is received at pin 63 of the I/O Control card. This signal is present for 100 milliseconds. (With power on, pressing the computer PRESET switch applies the POPIO signal to the I/O Control card for as long as the switch is pressed.) During the presence of the POPIO signal, the computer clock runs and continually repeats times T0 through T7 while remaining in Phase 1. When the POPIO signal drops, the computer is in Phase 1 and the initial conditions of the interface cards have been established for proper operation. The POPIO signal performs the following functions which are described in Paragraphs 3-6 through 3-9:

a. Disables the Interrupt System.

b. Provides a false Enable Service Request signal to the I/O Address card.

c. Sets the Flag Buffer and Flag FFs and resets the IRQ FF on all interface cards.

d. Resets the Control FF on all interface cards.

3-6. Disables the Interrupt System: The POPIO signal resets the Interrupt System Enable FF (MC87) through diode CR1, disabling the interrupt system. (The FF consists of two inverting "or" gates which are connected such that the FF can be reset by a true signal to either the reset-side input or the reset-side output of the FF.)

NOTE

Table 3-2 lists the part numbers of the Microcircuit Packages identified in Figure 3-2 by reference designations preceded by MC. Figure A-1 in Appendix A contains logic diagrams of the Microcircuit Packages according to part number.

3-7. Provides a False Enable Service Request Signal: When the Interrupt System Enable FF was reset, the true reset-side output of the FF is applied to the input of inverting "or" gate MC26A through diode CR3 The output of gate MC26A is a false Enable Service Request signal to the I/O Address card. This prevents the I/O Address card from sending an Interrupt signal to the computer which would switch the computer into Interrupt Phase 4.

3-8. Sets the Flag Buffer and Flag FFs and resets the IRQ (Interrupt Request) FF: The POPIO signal forms the buffered POPIO signal (POPIO (B)), through "and" gate MC107A, to set the Flag Buffer FF on all interface cards. At time T2, the T2 clock signal to the I/O Control card (through "and" gate MC77B) forms the ENF signal. This signal resets the IRQ FF on the interface cards and, with the set Flag Buffer FF output, sets the Flag FF on all interface cards.

3-9 Resets the Control FFs: The POPIO signal forms the CRS signal through "and" gate MC77A, to reset the Control FF on all interface cards and to reset the Interrupt Control FF (MC16) through diode CR2 on the I/O Control card. (The CRS signal can also be programmed by a CLC instruction with a Select Code of 00 (octal); see Paragraph 3-20.) Resetting the Control FFs prevents an interrupt from occurring when the interrupt system is initially enabled (Interrupt System Enable FF on the I/O Control card gets set). Resetting Interrupt Control FF MC16 ensures a false Enable Service Request signal to the I/O Address card when the POPIO signal drops. This prevents an interrupt from occurring until after time T7 of the first machine phase after the POPIO signal drops to permit the execution of at least one program instruction. (The reset-side

output of the Interrupt Control FF enables "and" gate MC57B to form the IAK signal at time T1 of Phase 1; the IAK signal has no affect on the interface cards during the presence of the POPIO signal.)

3-10. SIR SIGNAL

3-11. At each T5 clock time, the T5 signal is received by the I/O Control card from the computer (Figure 3-2). This signal is applied to all interface-card slot connectors through "and" gate MC67B. The SIR signal enables setting of the IRQ (Interrupt Request) FF on the interface cards to provide Flag and IRQ signals to the I/O Address card during an interrupt request.

3-12. PRIORITY-EFFECTING INSTRUCTIONS

3-13. Four instructions, STC, CLC, STF, and CLF, effect the priority structure of the Input/Output devices; whether a device can request an interrupt or not depends upon whether its interface-card Control FF is set or reset (STC, CLC) or its Flag FF is set or reset (STF, CLF). If a device cannot request an interrupt, all succeeding lower-priority devices assume a priority of one higher in the priority chain, and vice versa.

3-14. The four instructions also inhibit all interrupts during the machine phase in which they occur by removing the Enable Service Request signal to the I/O Address card. This prevents interrupts during entry and exit from subroutines. Also, a combination of two of the four instructions are normally the next-to-last instruction in a service subroutine processing an interrupt (the last being a JMP,I instruction to cause return to the main program or to an address in another service subroutine). If another Input/Output device could interrupt immediately after execution of these instructions (and before the JMP,I instruction), the possibility would exist that the first device may interrupt a second time before the JMP,I instruction is performed. In this event, the first main-program address (or the other service-subroutine address) stored in the beginning of the service subroutine would be destroyed, preventing a return to the main program or to the other service subroutine.

3-15. (Refer to Figure 3-2.) Whenever any of the four instructions are programmed, the STC, CLC, STF, and CLF signals are received by the I/O Control card and applied to one of the MC56A through MC56D isolator gates. The applicable gate output is then a true input to "and"

gate MC36C. The MC36C gate output becomes true on receipt of clock signal TS (pin 27) and the IOG signal at time T3 plus 80 nanoseconds from "and" gate MC67A.

3-16. The IOG signal from the computer is sent to the I/O Control card at time T3 of each machine phase that an I/O Group instruction is performed and is applied to one input of "and" gate MC67A. The other input to gate MC67A is the IOG signal which has been delayed by about 80 nanoseconds to eliminate any noise which may have been generated during its formation. (The delay is caused by inverting "or" gates MC66A and MC66B, resistor R3, and capacitor C3.) At the end of the delay, gate MC67A provides a true output to "and" gate MC36C and a buffered IOG signal to all interface card slots. The IOG(B) signal is an enabling signal for the I/O Group instruction and the Select Code transferred to the selected interface card.

3-17. The true output of gate MC36C is applied to "and" gate MC46B. The other input to gate MC46B is true due to the inversion of the false PH5 signal by inverting "or" gate MC26B. The true output of "and" gate MC46B resets the Interrupt Control FF. The true reset-side output of the Interrupt Control FF is applied to inverting "or" gate MC26A, removing the Enable Service Request signal to the I/O Address card. Interrupt signals will not now be enabled to the computer for the remainder of the current machine phase.

3-18. At time T7 of the current machine phase, the SPC signal sets Interrupt Timing FF MC117. At time T0, TS of the next machine phase, true T0 and TS signals are applied to "and" gate MC46A. The true output of gate MC46A resets the Interrupt Timing FF. The set-side output of this FF is applied to the Interrupt Control FF which is set at time T0, TS by the trailing (negative-going) edge of the pulse output of the Interrupt Timing FF. The false reset-side output of the Interrupt Control FF is inverted by inverting "or" gate MC26A, providing a true Enable Service Request input to the I/O Address card, and enabling Interrupt signals to the computer.

3-19. RESETTING CONTROL FFs

3-20. The Control FF on all interface cards can be reset by the CLC instruction with a Select Code of 00. The CLC signal enters the I/O Control card at pin 75 and is applied to "and" gate MC47B, as shown in Figure 3-2. The other input to gate MC47B is from the output of "and"

gate MC37C. This gate output is true when Select Code 00 (octal) is received at pins 36 and 38, and the output of the IOG "and" gate MC67A is true. The true output of "and" gate MC47B then applies a CRS signal to all interface card slots via pin 65. The CRS signal resets the Control FF on the interface cards to prevent an interrupt request from any Input/Output device.

3-21. PHASE OPERATION

3-22. INTERRUPT PHASE 4. During Phase 4, the PH4 signal and clock signal T3 are received by the I/O Control card as shown in Figure 3-2. The T3 signal provides a buffered time-T3 signal to all interface-card slot connectors through "and" gate MC57A. The gate MC57A output and the PH4 signal cause a true output from "and" gate MC36A to reset the Interrupt Control FF. The true output of the Interrupt Control FF is inverted by inverting "or" gate MC26A, removing the Enable Service Request signal to the I/O Address card. Interrupt signals will not now be enabled to the computer until after the program counter steps (time T7 of Fetch phase 1).

3-23. FETCH PHASE 1. At time T1 of Fetch Phase 1, directly following the Interrupt Phase, the PH1 signal and clock signal T1 are applied to "and" gate MC36B. The true output of gate MC36B is one input to "and" gate MC57B. The other input to gate MC57B is the true reset-side output of the Interrupt Control FF. Thus, gate MC57B provides a true IAK signal to all interface-card slot connectors. The IAK signal causes the Flag Buffer FF on the interface card which initiated the interrupt to be reset.

3-24. The Enable Service Request signal is inhibited from Interrupt Phase 4 until after time T7 of the Fetch Phase of the instruction in the computer-memory interrupt location unless further disabled by a JMP,I or JSB,I instruction in the interrupt location. This ensures full execution of at least one instruction before interrupts are again enabled. At time T7 of the Fetch phase, the SPC signal sets the Interrupt Timing FF. The FF is reset at time T0, TS of the next machine phase by the true output of "and" gate MC46A. The trailing-edge output of the Interrupt Timing FF sets the Interrupt Control FF at time T0, TS. The false reset-side output of the Interrupt Control FF is inverted by gate MC26A, providing a true Enable Service Request signal to the I/O Address card, and again enabling Interrupt signals to the computer.

3-25. DMA PHASE 5. When the Direct Memory Access (DMA) option is installed in the computer, DMA may hold up continuation of the computer program at the end of any machine phase for the purpose of transferring data. During the DMA operation, the computer is considered to be in Phase 5, although this phase is not one of the four basic computer phases. Phase 5 proceeds independently of any program which may be running. The I/O Control card receives two signals when the DMA operation is initiated; the HIS (Hold Interrupt System) signal and the PH5 signal. The HIS signal is applied to inverting "or" gate MC26A to remove the Enable Service Request signal to the I/O Address card. This prevents any normal Interrupt signal, from an Input/Output device interface card, from interrupting the computer. The PH5 signal is applied to inverting "or" gate MC26B to remove the I/O Address Enable signal to the I/O Address card. This prevents the normal 6-bit Select Code, which may be applied to the I/O Address card, from being decoded.

3-26. SWITCH AND OVERFLOW REGISTER SELECTION

3-27. Select Code 01 must be used to enter the computer Switch Register setting into the A or B Register when using Input/Output instructions LIA/B and MIA/B. Select Code 01 must also be used with Input/Output instructions STO, CLO, SOC, and SOS to perform operations using the 1-bit Overflow Register. Select Code 01 causes the SCM(0) and SCL(1) signals (Figure 3-2) to be applied to the I/O Control card "and" gate MC27C from the I/O Address card. The third input to gate MC27C is the IOG(B) signal, which became true at time T3. The true output of gate MC27C causes "and" gate MC47A to output the IOS signal. The IOS signal is sent to the computer to enable the applicable Switch Register or Overflow Register operations.

3-28. INTERRUPT SYSTEM CONTROL

3-29. The set or reset condition of the Interrupt System Enable FF (MC87) determines whether the interrupt system is "on" or "off", under program control. If the FF is set, the IEN signals to the interface cards will enable interrupt requests; if the FF is reset, the IEN signals are removed and interrupt requests will not be enabled. Initially, the interrupt system is disabled by the POPIO signal as described in Paragraph 3-6.

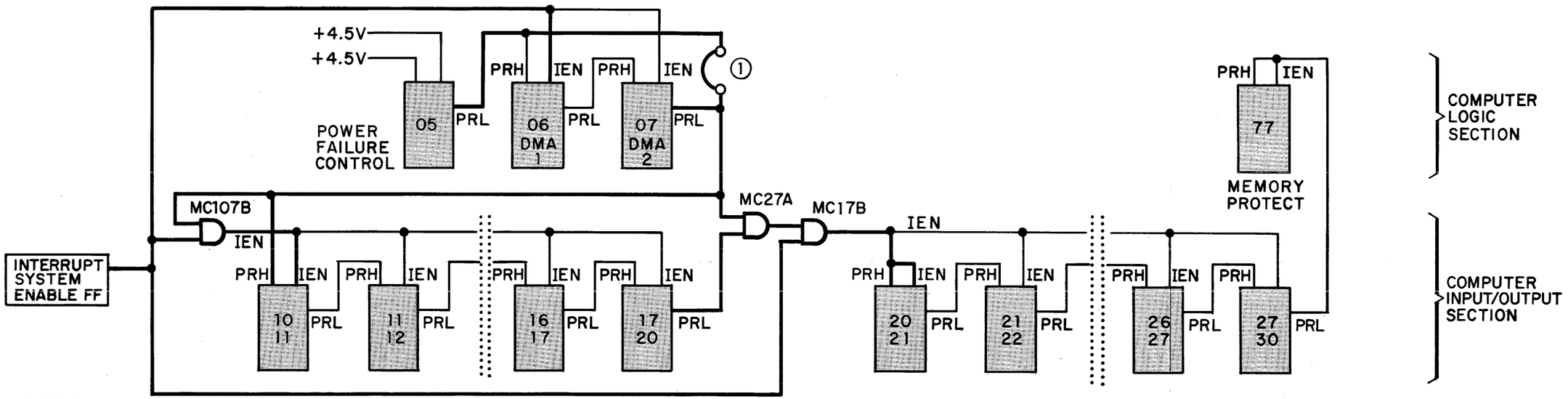
3-30. INTERRUPT SYSTEM ENABLE. If the interrupt system is to function, the Interrupt System Enable FF (Figure 3-2) must be set by a STF instruction with a Select Code of 00. When this is programmed, the SCM(0) and SCL(0) signals are received by the I/O Control card (from the I/O Address card) and applied to "and" gate MC37C. The remaining input to gate MC37C is the true IOG(B) signal. The true output of gate MC37C

is "anded" with the STF signal at "and" gate MC37A at time T3. The true output of gate MC37A sets the Interrupt System Enable FF.

3-31. The Enable Service Request signal is sent to the I/O Address card since both inputs to inverting "or" gate MC26A become false. One input is made false by the STF signal resetting FF MC16 through "and" gates MC56C, MC36C, and MC46B. The other input is made false by the false reset-side output of the Interrupt System Enable FF through diode CR3.

3-32. Refer to Figures 3-1 and 3-2. The true set-side output of the Interrupt System Enable FF is applied to "and" gate MC107B and through pin 10 to the interface-card slot connector with a Select Code of 06 as a true IEN(6) signal. Pin 10 is also connected to pin 5 of the I/O Control card by computer backplane wiring to apply a true input to one side of "and" gate MC17B. If the DMA option is not installed and there are no interrupt requests to the computer, the true PRL(5) signal from the Power Failure Control card is applied to pins 12 and 14. (If DMA is installed, the input to pins 12 and 14 is from PRL(7) and the line to PRL(5) must be opened.) The PRL(5) signal is also sent to the slot connector with a Select Code of 10 as a true PRH(10) signal. The PRL(5) signal applies a true input to "and" gate MC27A and causes "and" gate MC107B to apply a true IEN signal to the slot connector with a Select Code of 10. Since it is assumed that no interrupt requests are being made, the PRL(17) signal is true and the output of gate MC27A will be true. Both inputs to "and" gate MC17B are now true and its output will be sent to the interface-card slot connector with a lower Select Code of 20 as true IEN(20) and PRH(20) signals. As shown in Figure 3-1, the IEN(6) signal is jumpered to IEN(7); the IEN(10) signal is jumpered to IEN(11) through IEN(17); and IEN(20) is jumpered to IEN(21) through IEN(27). If both input and output logic is contained on one interface card, the IEN signal enters the card at pin 8 and is then transferred to both logic sections of the card. The entire interrupt system is now enabled and interrupt requests can be initiated.

3-33. INTERRUPT SYSTEM DISABLE. To disable the interrupt system, the Interrupt System Enable FF must be reset by a CLF instruction with a Select Code of 00. When this is programmed, the SCM(0) and SCL(0) signals are applied to "and" gate MC37C. Since the CLF instruction is an IOG instruction, the output of "and" gate MC67A (which is applied to gate MC37C) will be true about 80 nanoseconds after receipt of the IOG signal. All inputs to gate MC37C are then true. The true



NOTES:

① Remove Jumper when DMA Option is installed

2. Heavy lines denote I/O Control Card Signal Paths and Logic Elements.

Figure 3-1. I/O Control Card IEN, PRH, and PRL Signals

output of gate MC37C is applied to "and" gate MC37B. The true CLF signal is also applied to gate MC37B. The true output of this "and" gate resets the Interrupt System Enable FF. The set-side output of the FF becomes false, removing the IEN signal to all interface-card slot connectors (see Figure 3-1). This immediately prevents any interface card (device) from requesting an interrupt.

3-34. SKIP FLAG INSTRUCTIONS

3-35. Through the use of the SFS and SFC program instructions, the next instruction in the computer program can be skipped depending on the set or reset condition of the Interrupt System Enable FF. When the Interrupt System Enable FF is set and an SFS instruction is programmed with a Select Code of 00, all inputs to "and" gate MC97A are true. (The output of "and" gate MC37C is true since the SFS instruction is an IOG instruction and provides the IOG signal, and the SCM(0) and SCL(0) signals represent the Select Code used.) Gate MC97A causes "and" gate MC17A to issue a true SKF signal to the computer. The SKF signal causes the program to skip the next instruction since the Interrupt System Enable FF was set.

3-36. Similarly, when the Interrupt System Enable FF is reset and an SFC instruction is programmed with a Select Code of 00, all inputs to "and" gate MC97B are true (for the same reasons as in Paragraph 3-35). Gate MC97B causes "and" gate MC17A to issue a true SKF signal to the computer. The SKF signal again causes the program to skip the next instruction since in this case, the Interrupt System Enable FF was reset.

3-37. REPLACEABLE PARTS

3-38. Refer to Table 3-1 for a list of replaceable parts in alpha-numerical order of their reference designations, with a description and HP part number for each part.

3-39. To order a replacement part, address the order or inquiry to your local Hewlett-Packard field office. See the list at the rear of this manual for field-office addresses.

3-40. Specify the following information for each part when ordering:

a. Hewlett-Packard part number.
b. Circuit reference designation.
c. Description.

3-41. To order a part not listed in Table 3-1, give a complete description of the part and include its function and location.

Table 3-1. Replaceable Parts For I/O Control Card

REFERENCE DESIGNATION	DESCRIPTION	HP PART NO.
C1, C2	Capacitor, fixed, Tant., 2.2 μf	0180-0155
C3	Capacitor, fixed, ceramic, 300 pf	0140-0225
CR1, CR2, CR3	Diode	1910-0022
MC16	Microcircuit Package	1820-0957
MC17, MC47, MC57, MC67, MC77, MC107	Microcircuit Package	1820-0956
MC26, MC66, MC87, MC117	Microcircuit Package	1820-0952
MC27, MC36, MC37, MC46	Microcircuit Package	1820-0953
MC56	Microcircuit Package	1820-0965
MC97	Microcircuit Package	1820-0954
R1, R2, R4 thru R6	Resistor, fixed, 1k ±5%, 1/4 w	0683-1025
R3	Resistor, fixed, 1k ±5%	0757-0924

Notes for Figure 3-2, I/O Control Card Logic Diagram

1. Open connection to PRL(5) when DMA is installed and PRL(7) is connected.

2. All logic is positive-true unless otherwise specified.

3. Refer to text for the machine phases in which the signals in the timing chart occur.

4. A jumper replaces CR3 on D-640-6 Revision cards.

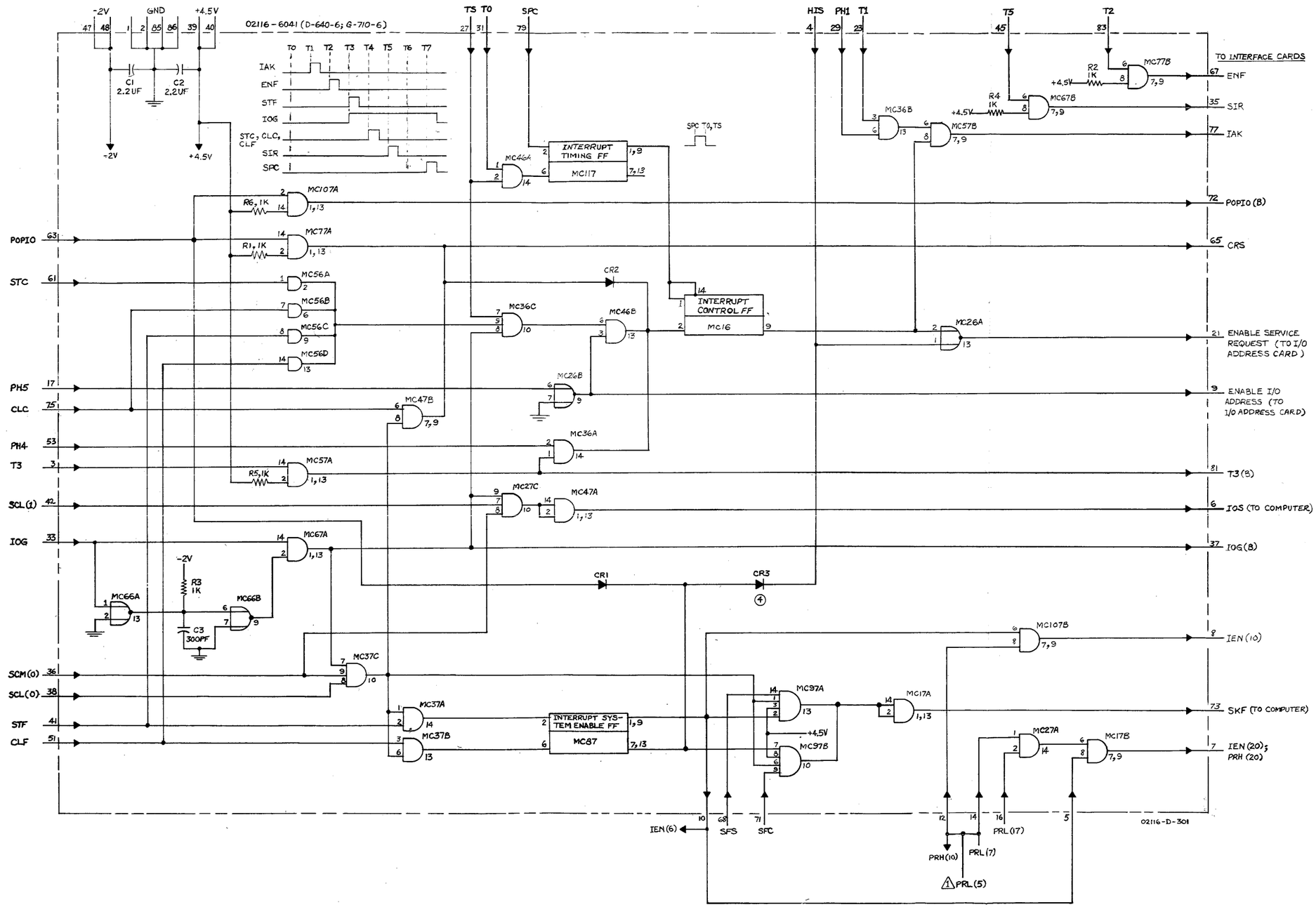


Figure 3-2. I/O Control Card Logic Diagram

SECTION IV

I/O ADDRESS CARD

4-1. INTRODUCTION

4-2. This section provides theory of operation information for the I/O Address card (HP Part No. 02116-6042). The card is of standard interface-card size and plugs into Position 202 on the left side of the Input/Output slots of the computer. The slot connector transfers all signals to and from the card; no additional cabling is required. The I/O Address card has two main functions. First, it decodes the 6-bit Select Code from the computer to provide a 2-digit octal code for selection of the interface card through which the computer is to communicate with the Input/Output device. Second, it encodes the Flag and and IRQ signals from the interface cards to provide a 6-bit address and an Interrupt signal to the computer. The 6-bit address identifies the interface card (device) requesting an interrupt.

4-3. THEORY OF OPERATION

4-4. DECODING FUNCTION

4-5. When an I/O instruction is programmed, the 6-bit Select Code portion (bits 0 through 5) of the instruction is received by the I/O Address card (Figure 4-2). The three least significant bits (0-2) and their NOT conditions are applied to eight "and" gates, MC55 A/B, MC65 A/B, MC75 A/B, and MC85 A/B. The three most significant bits (3-5) and their NOT conditions are also applied to eight "and" gates, MC95 A/B, MC105 A/B, MC115 A/B, and MC125A/B. All "and" gates have a common enabling input from "and" gate MC16A. The Enable I/O Address signal to gate MC16A is received from the I/O Control card and is always true except during Direct Memory Access (DMA) operations (Phase 5).

NOTE

Table 4-2 lists the part numbers of the Microcircuit Packages identified in Figure 4-2 by reference designations preceded by MC. Figure A-1 in Appendix A contains logic diagrams of the Microcircuit Packages according to part number.

4-6. The true output of each "and" gate represents an octal digit and only one "and" gate in each group of eight will be true for any given Select Code. The true outputs of the two "and" gates form the SCM (Select Code Most Significant Digit) and the SCL (Select Code Least significant digit) signals. Each of the outputs of this first group of 16 "and" gates are buffered out of the I/O Address card to the interface cards by a second group of 16 gates. These gates provide the drive necessary to apply signals of proper amplitude to the interface cards. The 1k resistor between each of the gates and the -2-volt supply minimizes the affect of any transient noise which may exist on the lines to the interface cards and reduces the fall time of the gate output voltage.

4-7. Example: With a Select Code of 11 (001 001 binary) applied to the I/O Address card, only bit 0 and bit 3 are true input signals. In Figure 4-2, each Select-Code bit input is applied to four "and" gates as follows:

a. The bit 0 input is applied to "and" gates MC75B, MC55B, MC65B, and MC85B. The output of "and" gate MC75B is true since the bit 0, bit $\overline{1}$, and bit $\overline{2}$ inputs and the output of gate MC16A are true inputs. The outputs of the other three "and" gates are false since the bit 1 and bit 2 inputs are false. The output of gate MC75B is applied to "and" gate MC76B and then to pin 67 as a true SCL(1) signal to the interface cards.

b. The bit 3 input is applied to "and" gates MC105B, MC95B, MC115B, and MC125B. The output of "and" gate MC125B is true since the bit 3, bit $\overline{4}$, and bit $\overline{5}$ inputs and the output of gate MC16A are true inputs. The outputs of the other three "and" gates are false since the bit 4 and bit 5 inputs are false. The output of gate MC125B is applied to "and" gate MC126B and then to pin 77 as a true SCM(1) signal to the interface cards.

4-8. The SCM and SCL signal combination determines the slot connector containing the interface card to which the instruction portion of the I/O instruction word is directed. Each slot connector, and therefore each interface card, contains two octal Select Codes as was described in Section II. Figure 4-1 illustrates the SCM and SCL signal paths to basic computer interface-card slot connectors. Note that the SCM(1) signal is applied to the most-significant-digit input pins on interface-card slot connectors with Select Codes of 10 through 17. The SCM(2) signal is applied to basic computer interface-card slot connectors with Select Codes of 20 through 27. Similarly, the SCM(3) through SCM(7) signals are applied to Module Extender options containing interface-card slot connectors with Select Codes

of 30 through 47, 50 through 67, and 70 through 77. The SCM(0) signal is applied to the I/O Control card (Select Codes 00 and 01) slot connector in the Input/Output section of the computer. It is also applied to the DMA 1 and DMA 2 option (Select Codes 02, 03, 06, and 07) and the Power Failure Control option (Select Code 05) slot connectors in the Logic section of the computer. The SCL(0) through SCL(7) signals are applied to the least-significant-digit input pins on the slot connectors in the computer and in the Module Extender options. The slot connectors in the Module Extender options are wired in the same manner as those in the basic computer.

4-9. The SCM and SCL signals are applied to the same-numbered pins on all interface-card slot connectors as follows:

a. Pin 14: Lower Select Code, Most Significant digit. (LSCM).

b. Pin 16: Lower Select Code, Least Significant digit. (LSCL).

c. Pin 37: Higher Select Code, Most Significant digit. (HSCM).

d. Pin 34: Higher Select Code, Least Significant digit. (HSCL).

4-10. ENCODING FUNCTION

4-11. When an Input/Output device requests an interrupt of the computer program, the IRQ FF on the interface card for the device is set. The set-side output of the IRQ FF applies a true FLG (Flag) signal to the I/O Address card; the reset-side output of the FF is inverted by an inverting "or" gate to apply a true IRQ signal to the I/O Address card. Refer to Figure 4-2. These two signals are used to form the Interrupt signal and the Service Request Address to be transferred to the computer.

4-12. INTERRUPT SIGNAL. An Interrupt signal is sent to the computer at time T5 of the current machine phase when a Flag signal is received from an interface card and if the Enable Service Request signal is received from the I/O Control card. (To establish when the Enable Service Request signal is true, refer to Figure 2-6, Typical Interrupt System Timing.) The Interrupt signal causes the computer to enter Interrupt Phase 4 at the end of the current machine phase.

4-13. As shown in Figure 4-2, four Flag signals (0 through 3) can be received from the interface cards. These signals are described in steps "a" through "d". Receipt of a Flag signal applies a true input to "and" gate MC16B through one of the CR33 through CR36 diodes. If the Enable Service Request signal is true, the gate MC16B output is applied to the computer as a true Interrupt signal.

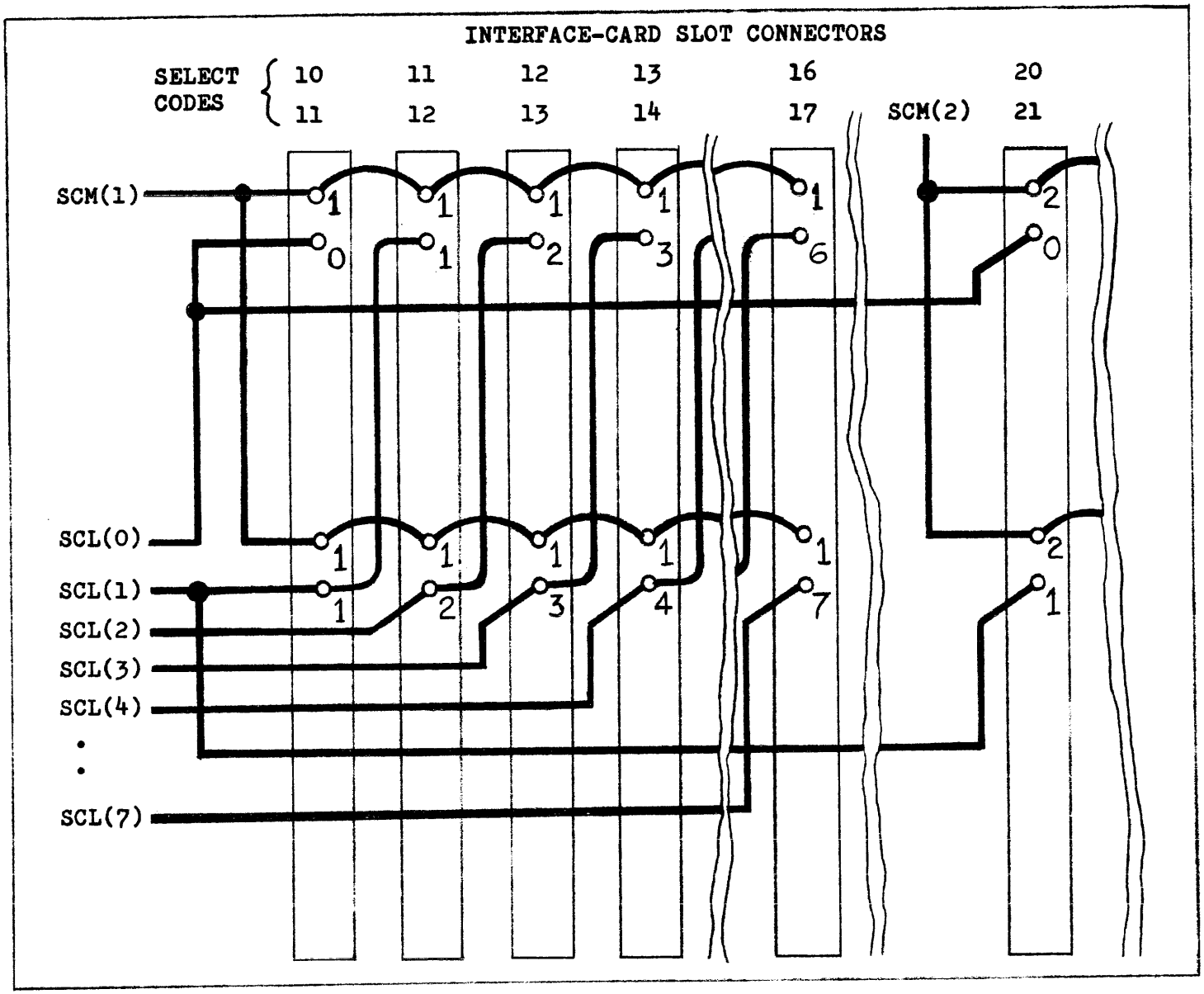


Figure 4-1. SCM and SCL Signal Paths

a. Flag (0): This input is true when an interface card with a Select Code of 05 to 17 is requesting an interrupt.

b. Flag (1): This input is true when an interface card with a Select Code of 20 to 37 is requesting an interrupt.

c. Flag (2): This input is true when an interface card with a Select Code of 40 to 57 is requesting an interrupt.

d. Flag (3): This input is true when an interface card with a Select Code of 60 to 77 is requesting an interrupt.

4-14. SERVICE REQUEST ADDRESS. Refer to Figure 4-2. The 6-bit Service Request Address is the Select Code of the interface card requesting an interrupt, in binary form. It is sent to the M-register of the computer via the T bus and specifies the interrupt location for that device in memory. (The interrupt location contains the instruction to be executed when the particular interrupt occurs.) While the Interrupt signal is sent to the computer at time T5 of the current machine phase, the Service Request Address is not enabled to the computer until time T7 of Interrupt Phase 4.

4-15. The Service Request Address is formed by encoding the combination of Flag and IRQ signals from the interface card requesting an interrupt. The Flag signals are true for the conditions listed in Paragraph 4-13 steps "a" through "d". The Flag (1) through Flag (3) signals determine the two most significant bits (bits 4 and 5) of the address and are applied to diodes CR37 through CR40 and then to "and" gates MC17A and MC17B. The Flag(0) signal has no affect on the Service Request Address since it is received only from interface cards with Select Codes of 05 (000 101 binary) to 17 (001 111 binary), where bits 4 and 5 are always zero (false); see Paragraph 4-13, step "a". The IRQ signals determine the four least significant bits (bits 0 through 3) of the address and are applied to diodes CR1 through CR32 and then to "and" gates MC26A, MC26B, MC27A, and MC27B. The remaining input to the Service Request Address "and" gates is applied at time T7 of Interrupt Phase 4 by the RSM(IMC)6-9 signal from the computer.

4-16. Table 4-1 indicates the Flag and IRQ signals received from various interface cards identified by their Select Codes. It also indicates the I/O Address card components that these signals are applied to in obtaining the 6-bit Service Request Address. This table should be used in conjunction with Figure 4-2 to obtain an understanding of the encoding function of the I/O Address card.

Table 4-1. I/O Address Card Encoding Examples

Interface Card Select Code (Octal)	Flag Signal	Flag Signal is Applied		IRQ Signal	IRQ Signal is Applied		For a Service Req. Address of (Binary)
		To Diode(s)	Then to "and" Gate(s)		To Diode(s)	Then to "and" Gate(s)	
07	0	-	-	7	CR28, CR20, CR12	MC27B, MC27A MC26B	000 111
10	0	-	-	10	CR1	MC26A	001 000
21	1	CR38	MC17B	1	CR25	MC27B	010 001
32	1	CR38	MC17B	12	CR21, CR3	MC27A, MC26A	011 010
43	2	CR39	MC17A	3	CR26, CR18	MC27B, MC27A	100 011
54	2	CR39	MC17A	14	CR13, CR5	MC26B, MC26A	101 100
65	3	CR37, CR40	MC17B, MC17A	5	CR27, CR10	MC27B, MC26B	110 101
76	3	CR37, CR40	MC17B, MC17A	16	CR23, CR15, CR7	MC27A, MC26B MC26A	111 110

4-17. REPLACEABLE PARTS

4-18. Refer to Table 4-2 for a list of replaceable parts in alpha-numerical order of their reference designations, with a description and HP part number for each part.

4-19. To order a replacement part, address the order or inquiry to your local Hewlett-Packard field office. See the list at the rear of this manual for field-office addresses.

4-20. Specify the following information for each part when ordering:

a. Hewlett-Packard part number.

b. Circuit reference designation.

c. Description.

4-21. To order a part not listed in Table 4-2, give a complete description of the part and include its function and location.

Table 4-2. Replaceable Parts For I/O Address Card

REFERENCE DESIGNATION	DESCRIPTION	HP PART NO.
C1, C2	Capacitor, fixed, Tant., 2.2 μf	0180-0155
CR1 thru CR40	Diode	1901-0040
MC16, MC17, MC26, MC27, MC56, MC66, MC76, MC86, MC96, MC106, MC116, MC126	Microcircuit Package	1820-0956
MC55, MC65, MC75, MC85, MC95, MC105, MC115, MC125	Microcircuit Package	1820-0954
R1	Resistor, fixed, 470 ohms ±5%, 1/4 w	0683-4715
R2 thru R17	Resistor, fixed, 1k ±5%, 1/4 w	0683-1025

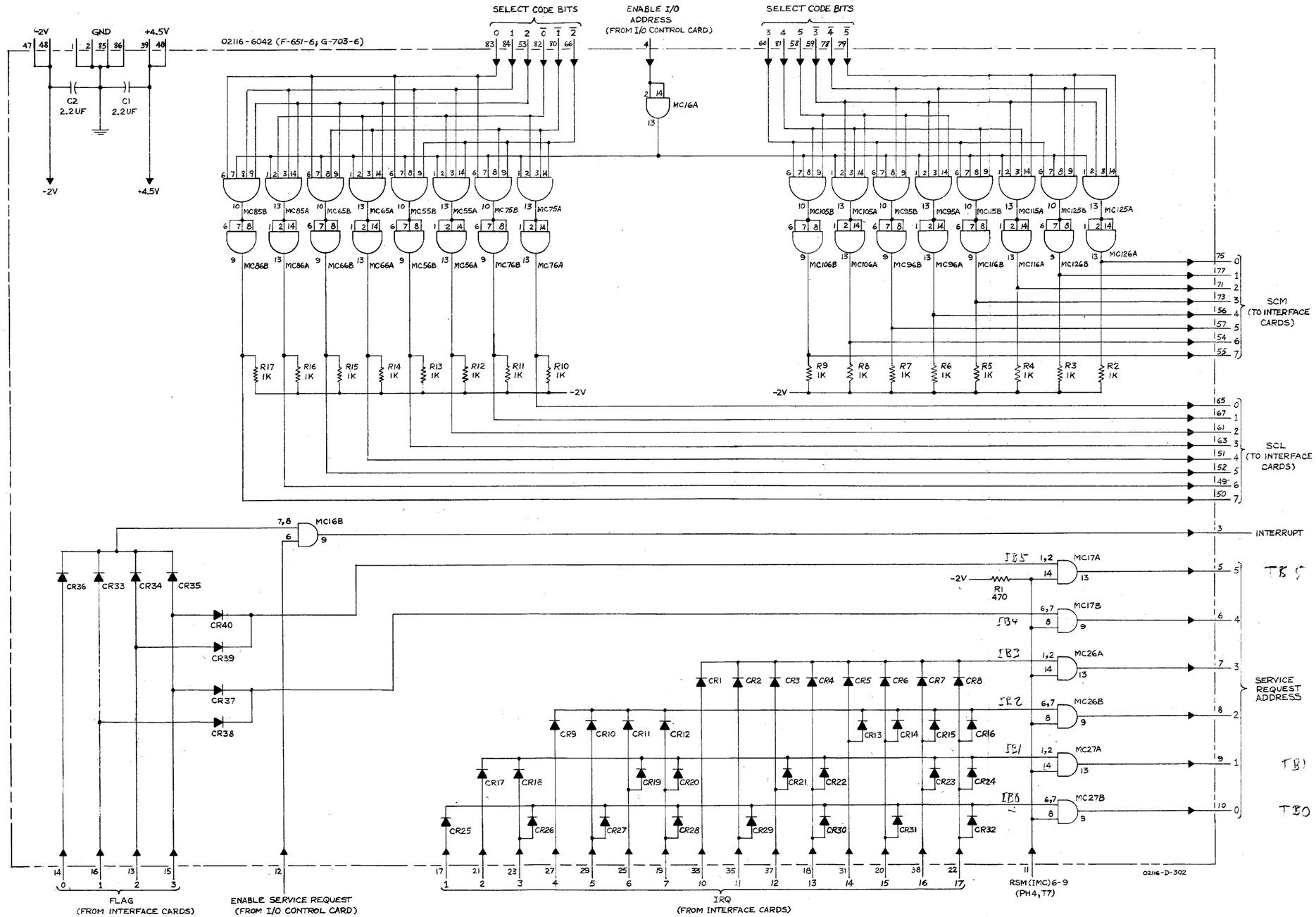


Figure 4-2. I/O Address Card Logic Diagram

SECTION V

RESISTANCE LOAD CARD

5-1. INTRODUCTION

5-2. This section contains description, installation and replaceable parts information, and a schematic diagram for the Resistance Load Card.

5-3. DESCRIPTION

5-4. The Resistance Load card (HP Part No. 02116-6047) is of standard interface-card size and plugs into Position 218 on the right side of the Input/Output slots of the computer. The card contains 17 resistors which are used to load the termination of the IOBO (I/O Bus Output) lines from the computer to the interface card slot connectors. These lines terminate at slot position 218. The other end of the resistors are connected to the -2-volt supply through slot connector pins 47 and 48. The lines are loaded to eliminate any transient noise generated by these lines in the backplane wiring of the computer. No external cabling to the Resistance Load card is required.

5-5. INSTALLATION

5-6. Pull open the front panel of the computer. Plug the Resistance Load card into slot position 218 of the computer Input/Output section. Close the front panel of the computer. The card remains in the computer unless the total interface and Priority Jumper cards equal 16. At that time, remove the card as it is no longer required.

NOTE

The Resistance Load card does not contain a priority bus circuit. Therefore it cannot be plugged into a slot with a lower slot-position number than one containing an interface or Priority Jumper card. If it is, the interrupt system of the computer will not function properly.

5-7. SCHEMATIC DIAGRAM

5-8. Refer to Figure 5-1 for a schematic diagram of the Resistance Load card.

5-9. REPLACEABLE PARTS

5-10. Refer to Table 5-1 for a list of replaceable parts in alpha-numerical order of their reference designations, with a description and HP part number for each part.

5-11. To order a replacement part, address the order or inquiry to your local Hewlett-Packard field office. See the list at the rear of this manual for field-office addresses.

5-12. Specify the following information for each part when ordering:

a. Hewlett-Packard part number.

b. Circuit reference designation.

c. Description.

5-13. To order parts not listed in Table 5-1, give a complete description of the part and include its function and location.

Table T5-1. Replaceable Parts for Resistance Load Card.

REFERENCE DESIGNATION	DESCRIPTION	HP PART NO.
R35, R38, R41, R43 R45, R51 thru R58, R61, R65, R73, R74	Resistor, fixed, 150 ohms	0683-1515

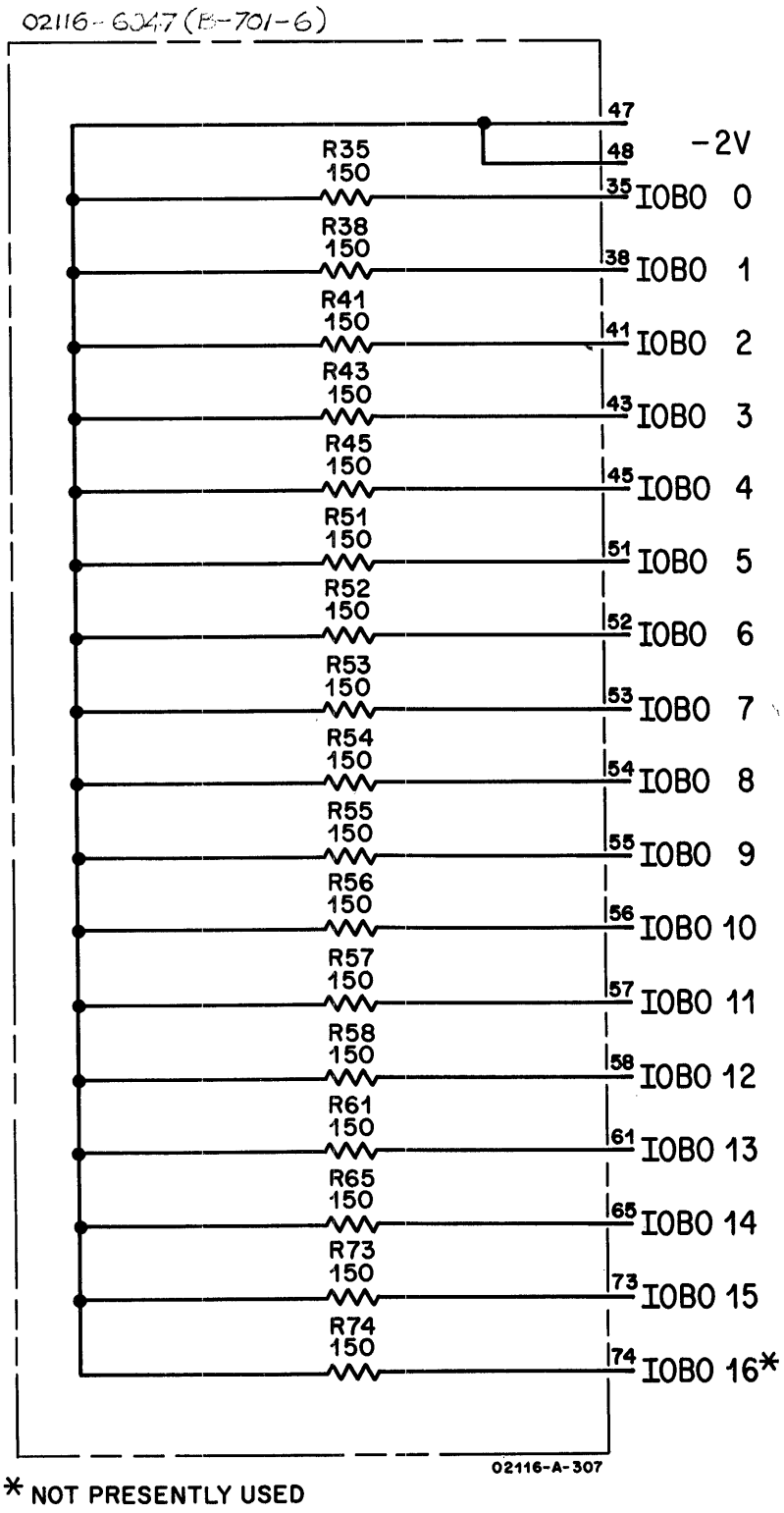
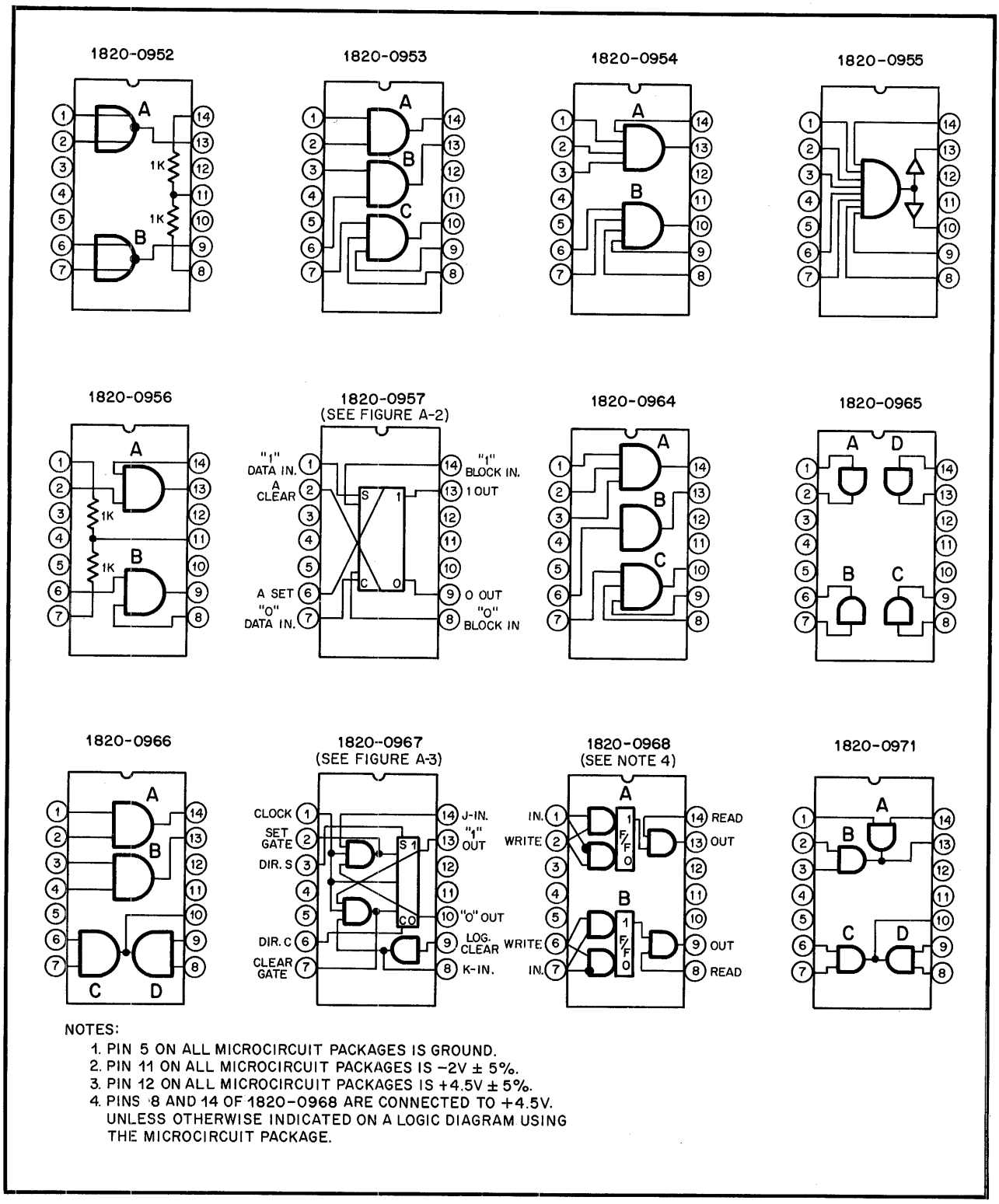


Figure 5-1. Resistance Load Card Schematic Diagram



NOTES:

1. PIN 5 ON ALL MICROCIRCUIT PACKAGES IS GROUND.
2. PIN 11 ON ALL MICROCIRCUIT PACKAGES IS −2V ± 5%.
3. PIN 12 ON ALL MICROCIRCUIT PACKAGES IS +4.5V ± 5%.
4. PINS 8 AND 14 OF 1820-0968 ARE CONNECTED TO +4.5V. UNLESS OTHERWISE INDICATED ON A LOGIC DIAGRAM USING THE MICROCIRCUIT PACKAGE.

Figure A-1. Logic Diagrams for Microcircuit Packages, Top View

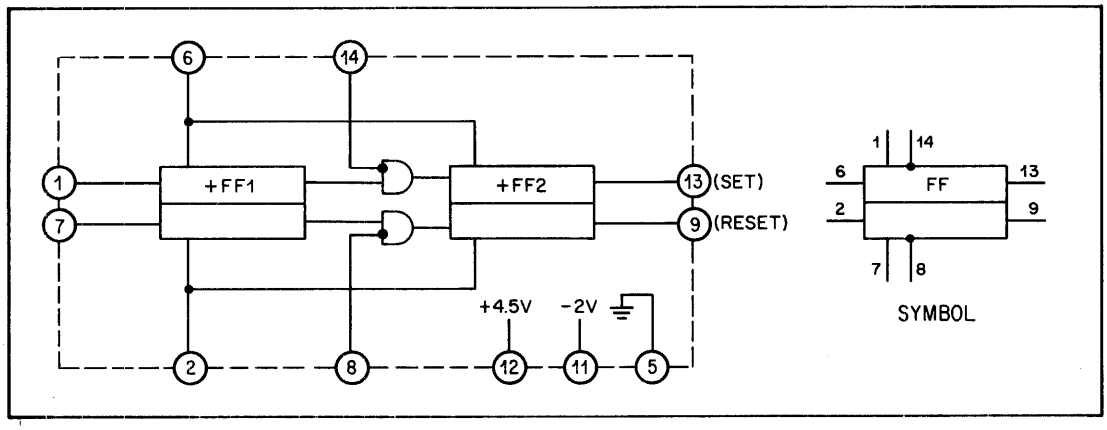
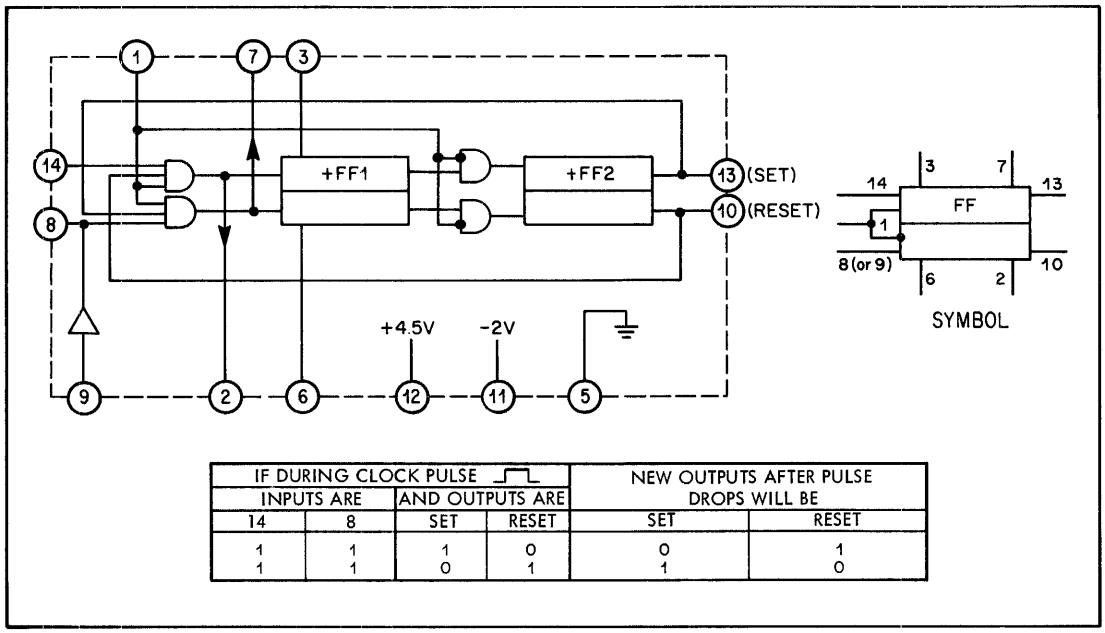


Figure A-2. Simplified Logic Diagram of 1820-0957 Microcircuit Package



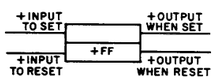
IF DURING CLOCK PULSE ⎍ INPUTS ARE		AND OUTPUTS ARE		NEW OUTPUTS AFTER PULSE DROPS WILL BE	
14	8	SET	RESET	SET	RESET
1	1	1	0	0	1
1	1	0	1	1	0

Figure A-3. Simplified Logic Diagram of 1820-0967 Microcircuit Package

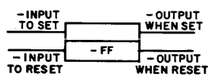
KEY TO LOGIC SYMBOLOGY

FLIP-FLOP

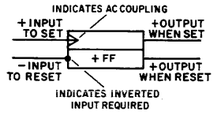
POSITIVE SET



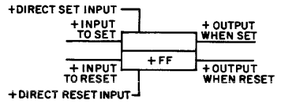
NEGATIVE SET



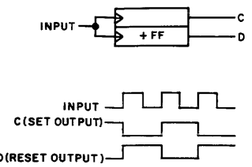
MIXED INPUT (POSITIVE SET SHOWN)



MULTIPLE INPUT (POSITIVE SET SHOWN)



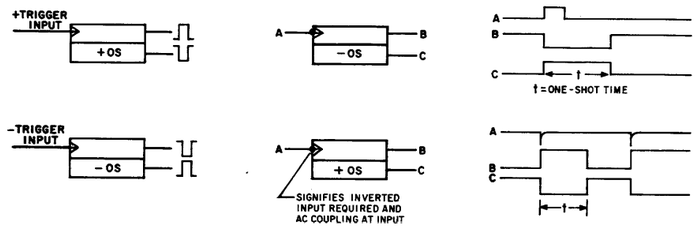
BINARY DIVIDER (USED FOR COUNTING)



NOTE:

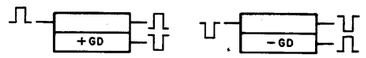
SET AND RESET INPUTS MAY BE INTERCHANGED, WITH THE RESET INPUT/OUTPUT LINES ABOVE THE SET INPUT/OUTPUT LINES.

ONE-SHOT



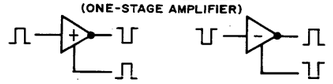
GATE DRIVER

(TWO-STAGE AMPLIFIER)



PHASE SPLITTER

(ONE-STAGE AMPLIFIER)



'AND' GATES

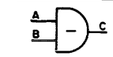
GATES WITH DC INPUT

POSITIVE TRUE

ALL INPUTS (A AND B) TRUE (+) MAKES OUTPUT (C) TRUE (+)

ANY INPUT (A OR B) FALSE (-) MAKES OUTPUT (C) FALSE (-)

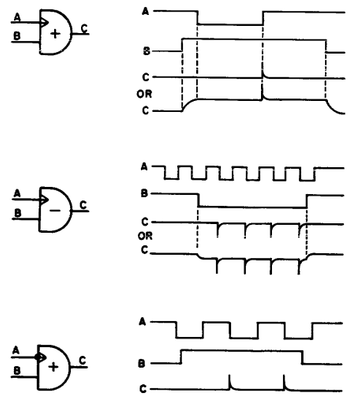
NEGATIVE TRUE



ALL INPUTS (A AND B) TRUE (-) MAKES OUTPUT (C) TRUE (-)

ANY INPUT (A OR B) FALSE (+) MAKES OUTPUT (C) FALSE (+)

GATES WITH AC INPUT

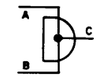


MIXED

A FALSE AND B TRUE MAKES OUTPUT TRUE

A TRUE OR B FALSE MAKES OUTPUT FALSE

WIRED 'AND'

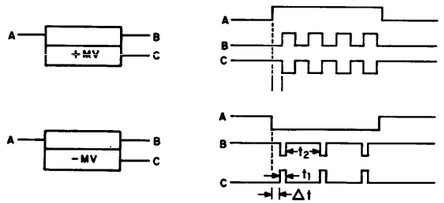


ELECTRICAL CONNECTION THAT ACTS AS AN 'AND' GATE

NOTE:

'AND' GATES MAY HAVE ANY NUMBER OF INPUTS; THE OUTPUT WILL BE PRODUCED ACCORDING TO THE RULES STATED HERE

ASTABLE MULTIVIBRATOR

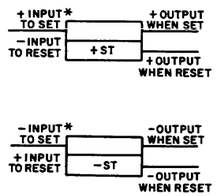


A IS INPUT REQUIRED FOR OPERATION; CORRESPONDS TO POLARITY (+MV OR -MV)

Δt IS DELAY OF FIRST TRANSITION

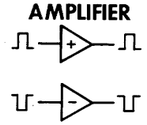
t_1-t_2 RATIO IS DETERMINED BY CIRUIT CONSTANTS

SCHMITT TRIGGER

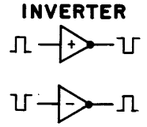


* WITH RESPECT TO REFERENCE LEVEL

AMPLIFIER



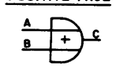
INVERTER



'OR' GATES

GATES WITH DC INPUT

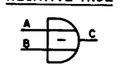
POSITIVE TRUE



INPUT (A OR B) TRUE (+) MAKES OUTPUT (C) TRUE (+)

ALL INPUTS FALSE (-) MAKES OUTPUT (C) FALSE (-)

NEGATIVE TRUE



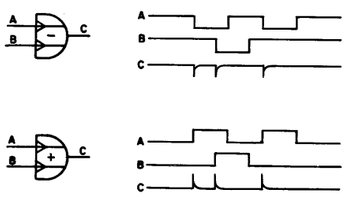
INPUT (A OR B) TRUE (-) MAKES OUTPUT (C) TRUE (-)

ALL INPUTS FALSE (-) MAKES OUTPUT (C) FALSE (-)

WIRED 'OR'

ELECTRICAL CONNECTION THAT ACTS AN 'OR' GATE

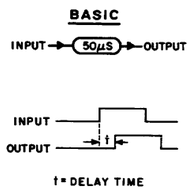
GATES WITH AC INPUT



NOTE: 'OR' GATES MAY HAVE ANY NUMBER OF INPUTS; THE OUTPUT WILL BE PRODUCED ACCORDING TO THE RULES STATED HERE

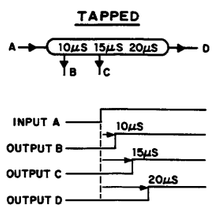
DELAY ELEMENTS

BASIC

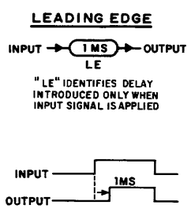


t = DELAY TIME

TAPPED

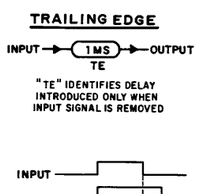


LEADING EDGE



"LE" IDENTIFIES DELAY INTRODUCED ONLY WHEN INPUT SIGNAL IS APPLIED

TRAILING EDGE



"TE" IDENTIFIES DELAY INTRODUCED ONLY WHEN INPUT SIGNAL IS REMOVED

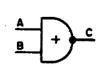
LEGEND

- + = POSITIVE TRUE
- − = NEGATIVE TRUE
- → = INFORMATION FLOW
- $\sqcap_{TE}$ = POSITIVE-GOING TRAILING EDGE (TRIGGER IDENTIFICATION)
- $\sqcup_{TE}$ = NEGATIVE-GOING TRAILING EDGE (TRIGGER IDENTIFICATION)
- = POLARITY INVERSION
- = INVERTED INPUT REQUIRED
- = AC COUPLING AT INPUT
- = INVERTED AC INPUT
- = INVERTED OUTPUT

NOTE: 'NOT' FUNCTIONS ARE SYMBOLIZED BY AN OVERSCORE. (e.g., $\overline{\text{VOLTS}}$ = NOT VOLTS)

'NAND' GATE

(POSITIVE-TRUE SHOWN)



ALL INPUTS (A AND B) TRUE (+) MAKES OUTPUT (C) FALSE (-)

ANY INPUT (A OR B) FALSE (-) MAKES OUTPUT (C) TRUE (+)

'NOR' GATE

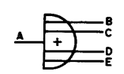
(POSITIVE-TRUE SHOWN)

ANY INPUT (A OR B) TRUE (+) MAKES OUTPUT (C) FALSE (-)

ALL INPUTS FALSE (-) MAKES OUTPUT (C) TRUE (+)

ENCODE GATE

(POSITIVE-TRUE SHOWN)

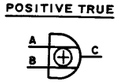


INPUT (A) TRUE (+) MAKES ALL OUTPUTS (B,C,D,E) TRUE (+)

INPUT (A) FALSE (-) MAKES ALL OUTPUTS (B,C,D,E) OPEN

EXCLUSIVE 'OR' GATE

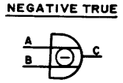
POSITIVE TRUE



ONE INPUT (A OR B) TRUE (+) MAKES OUTPUT (C) TRUE (+)

BOTH INPUTS (A AND B) TRUE (+) OR FALSE (-) MAKES OUTPUT (C) FALSE (-)

NEGATIVE TRUE



ONE INPUT (A OR B) TRUE (-) MAKES OUTPUT (C) TRUE (-)

BOTH INPUTS (A AND B) TRUE (-) OR FALSE (+) MAKES OUTPUT (C) FALSE (+)

NOTE: THIS IS A SUMMARY OF DETAILED DESCRIPTIONS AVAILABLE FROM DYMEC. ASK YOUR NEAREST HEWLETT-PACKARD SERVICE OFFICE FOR THE LOGIC SYMBOLOGY BOOKLET.